SCE 0110 -
Elementos de Lógica Digital I

Tecnologia de Implementação

Prof. Vanderlei Bonato

Sumário

- Como os transistores operam e formam comutadores/chaves simples
- Tecnologia de CI (Circuito Integrado)
- Portas lógicas CMOS

V_{DD} = V_{CC}/positivo/tensão da fonte de alimentação (1 a 5V)

V_{ss} = Gnd/negativo/ terra/comun (0V)

$V_{0,max}$ = tensão máxima para nível lógico 0

$V_{1, min}$ = tensão mínima para nível lógico 1

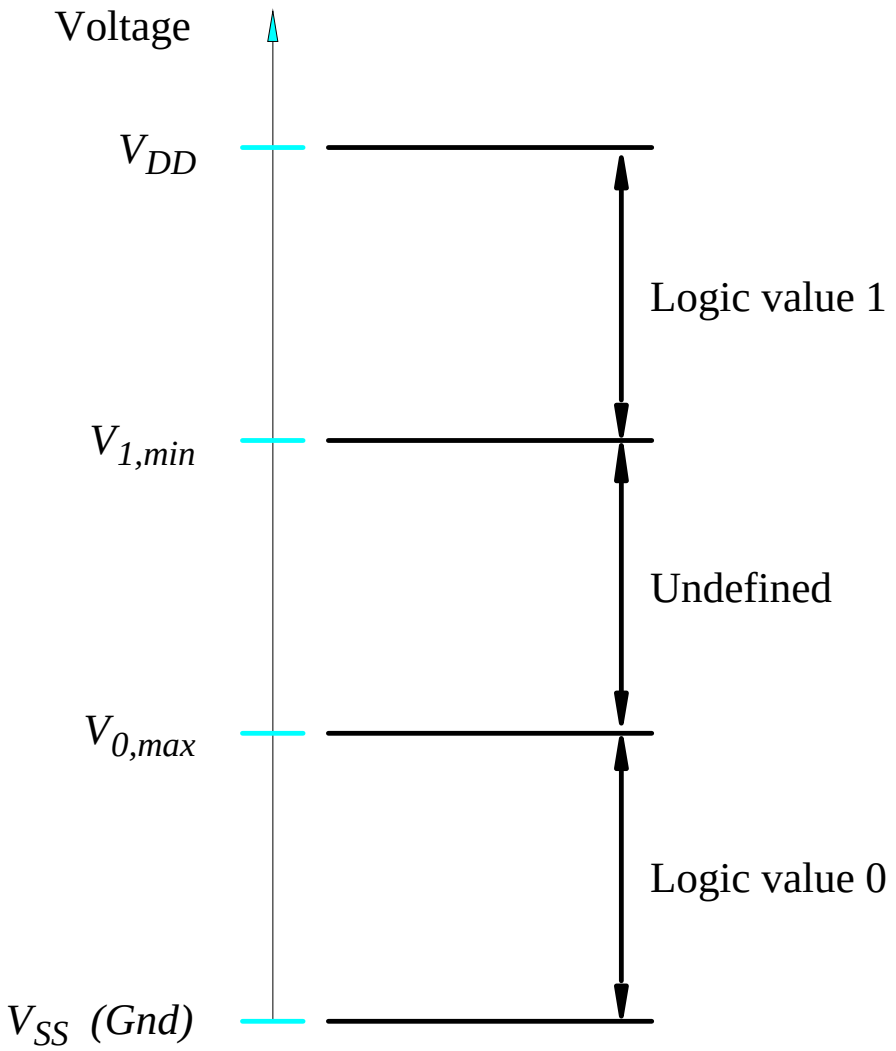
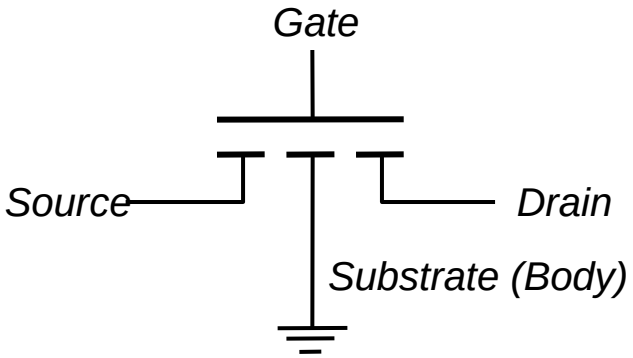


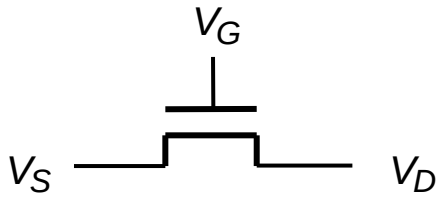
Figure 3.1. Logic values as voltage levels.

MOSFET (Metal Oxide Semiconductor Field-Effect Transistor): NMOS (Canal N)

(a) A simple switch controlled by the input *x*



(b) NMOS transistor

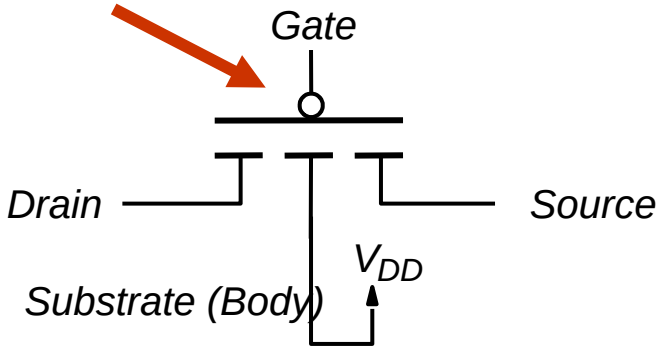


(c) Simplified symbol for an NMOS transistor

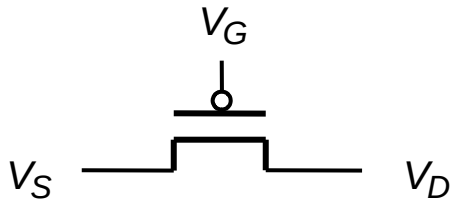
Figure 3.2. NMOS transistor as a switch.

MOSFET (Metal Oxide Semiconductor Field-Effect Transistor): PMOS (Canal P)

(a) A switch with the opposite behavior of Figure 3.2*a*



(b) PMOS transistor



(c) Simplified symbol for a PMOS transistor

Figure 3.3. PMOS transistor as a switch.

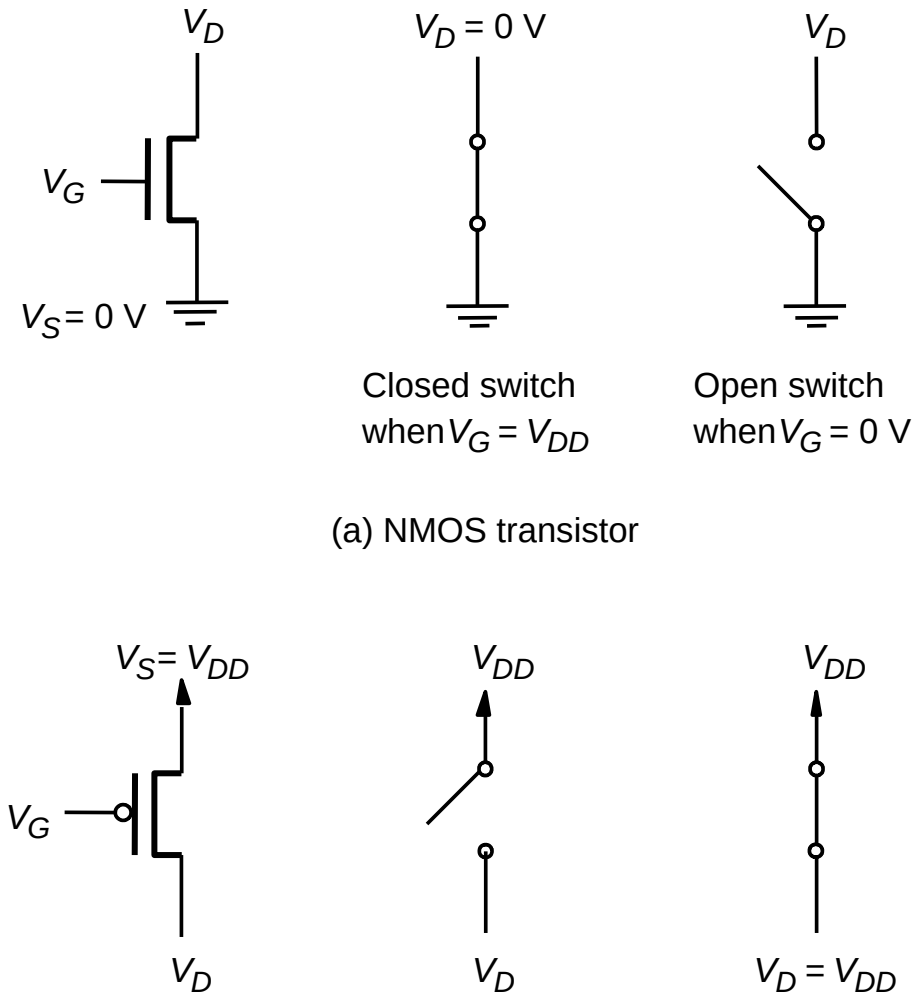
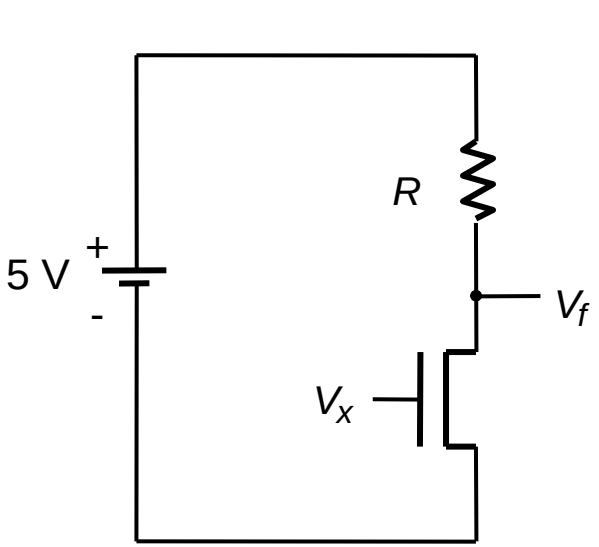


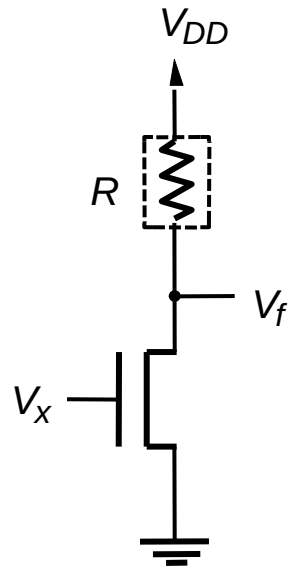
Figure 3.4. NMOS and PMOS transistors in logic circuits.

Histórico

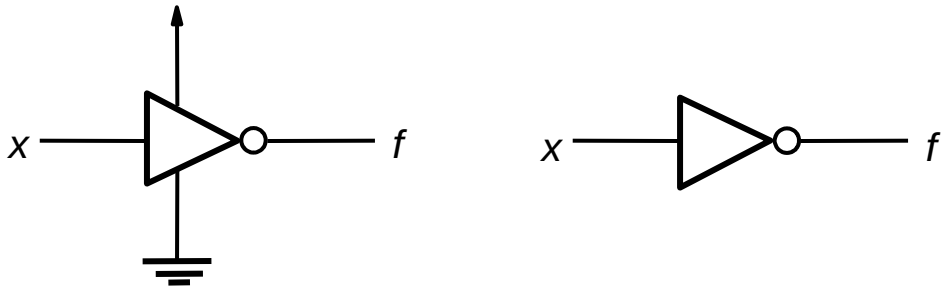
- A construção de portas lógicas com MOSFET tornou-se popular nos anos 70
- Nessa época utilizava-se NMOS ou PMOS, mas não ambas
- Desde os anos 80 passou-se a utilizar uma combinação de NMOS e PMOS, conhecida como CMOS (Complementary MOS)



(a) Circuit diagram

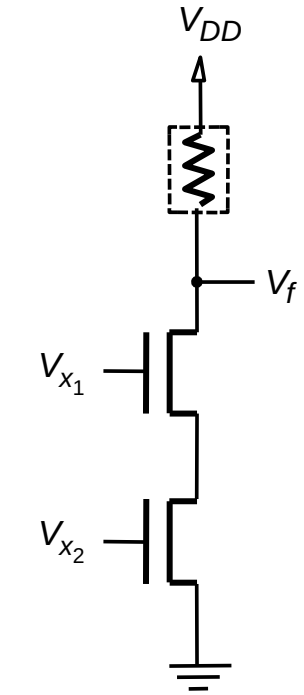


(b) Simplified circuit diagram



(c) Graphical symbols

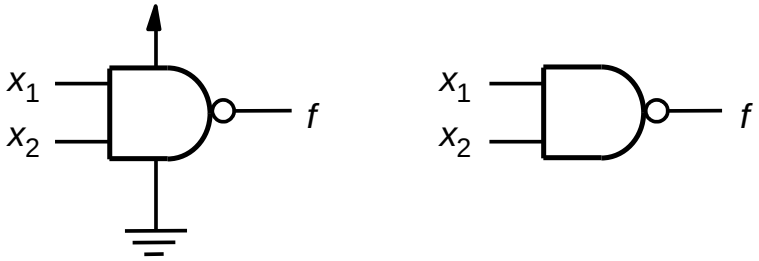
Figure 3.5. A NOT gate built using NMOS technology.



(a) Circuit

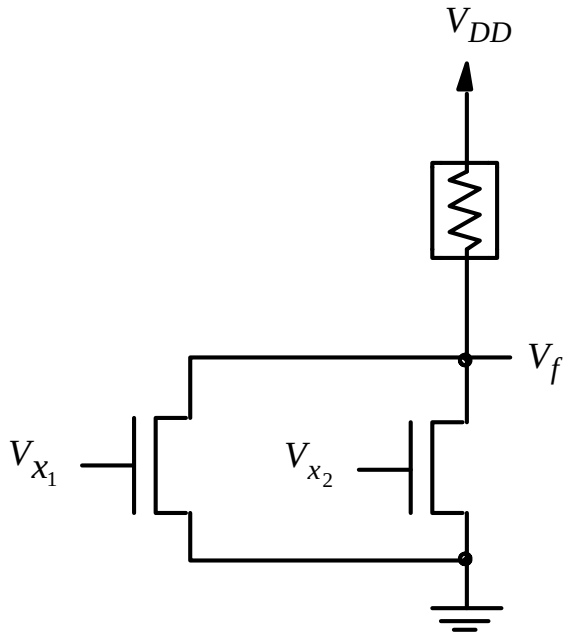
x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table



(c) Graphical symbols

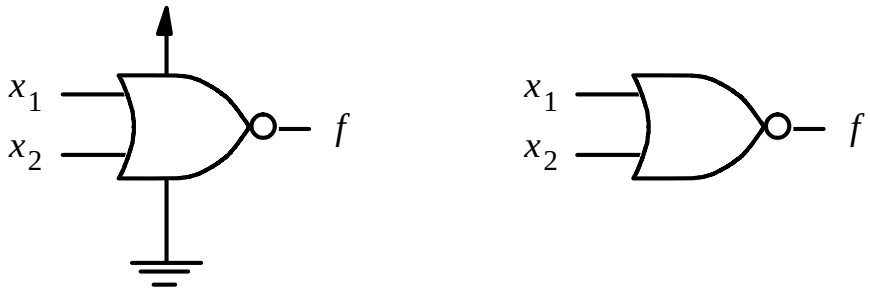
Figure 3.6. NMOS realization of a NAND gate.



(a) Circuit

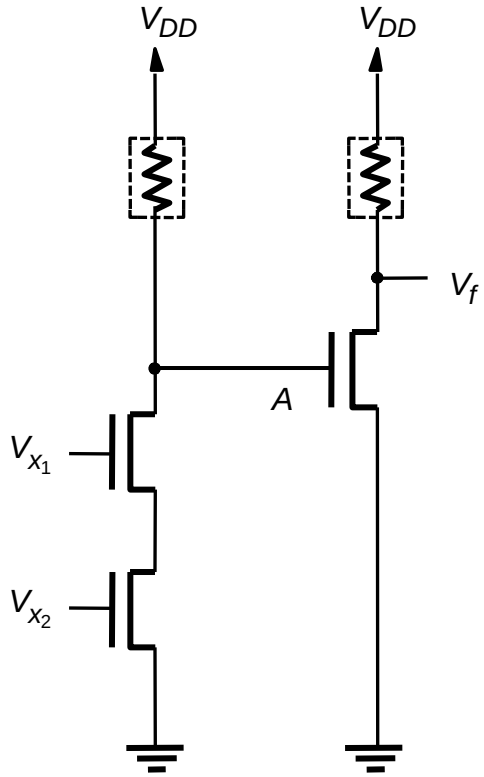
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



(c) Graphical symbols

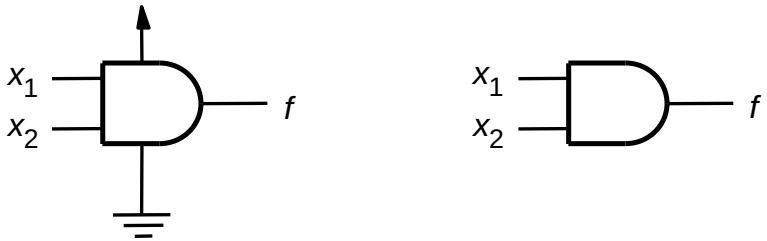
Figure 3.7. NMOS realization of a NOR gate.



(a) Circuit

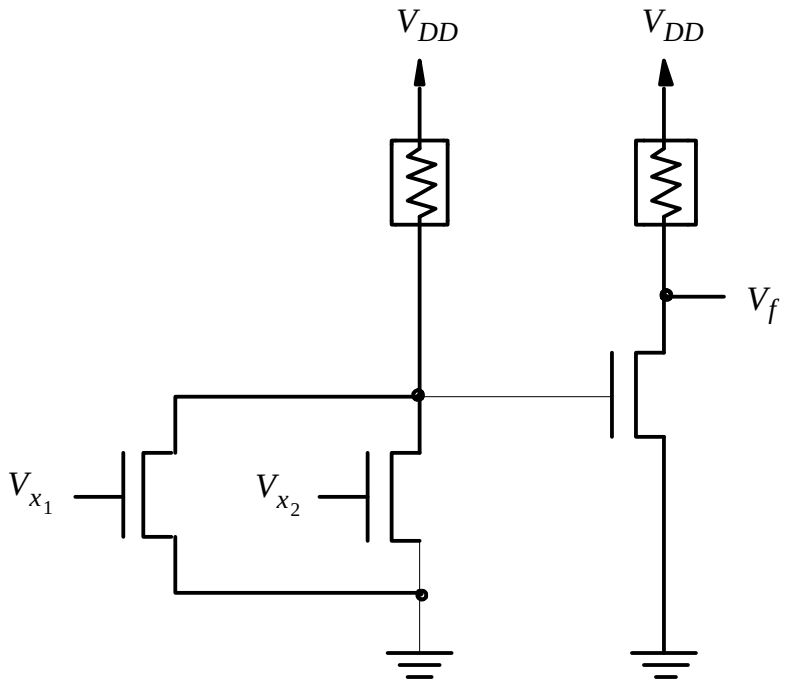
x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbols

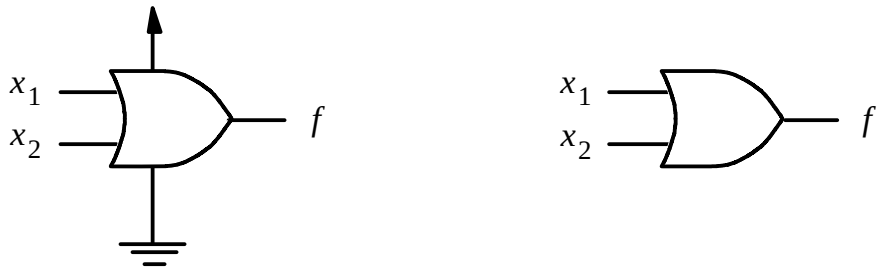
Figure 3.8. NMOS realization of an AND gate.



(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table



(c) Graphical symbols

Figure 3.9. NMOS realization of an OR gate.

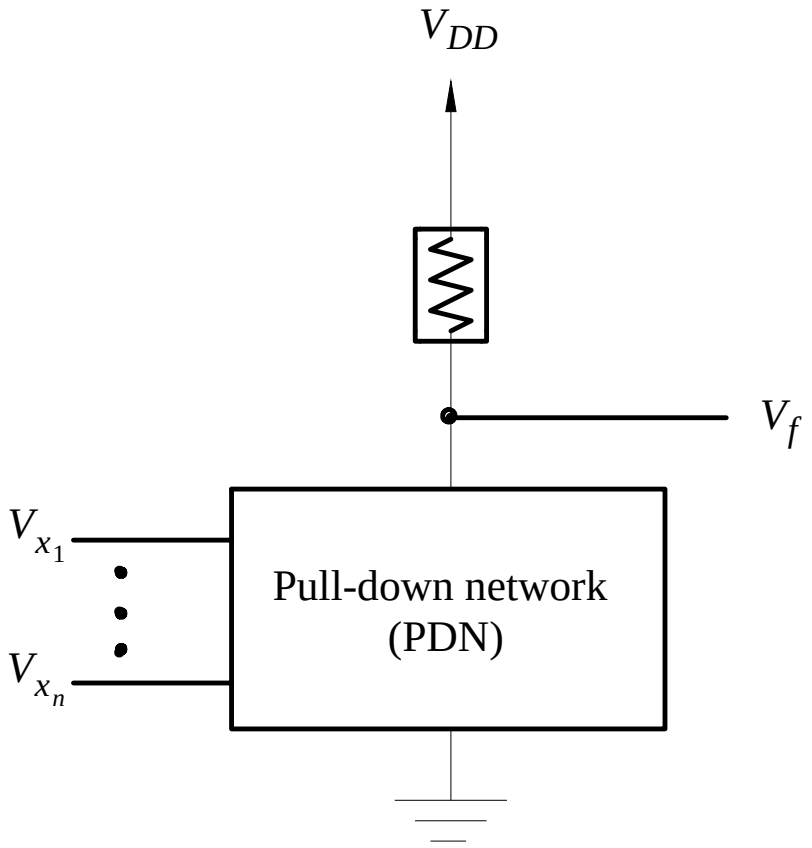


Figure 3.10. Structure of an NMOS circuit.

O conceito de circuitos CMOS é baseado na troca do dispositivo “pull-up” (resistores ligados ao Vcc) por transistores PMOS

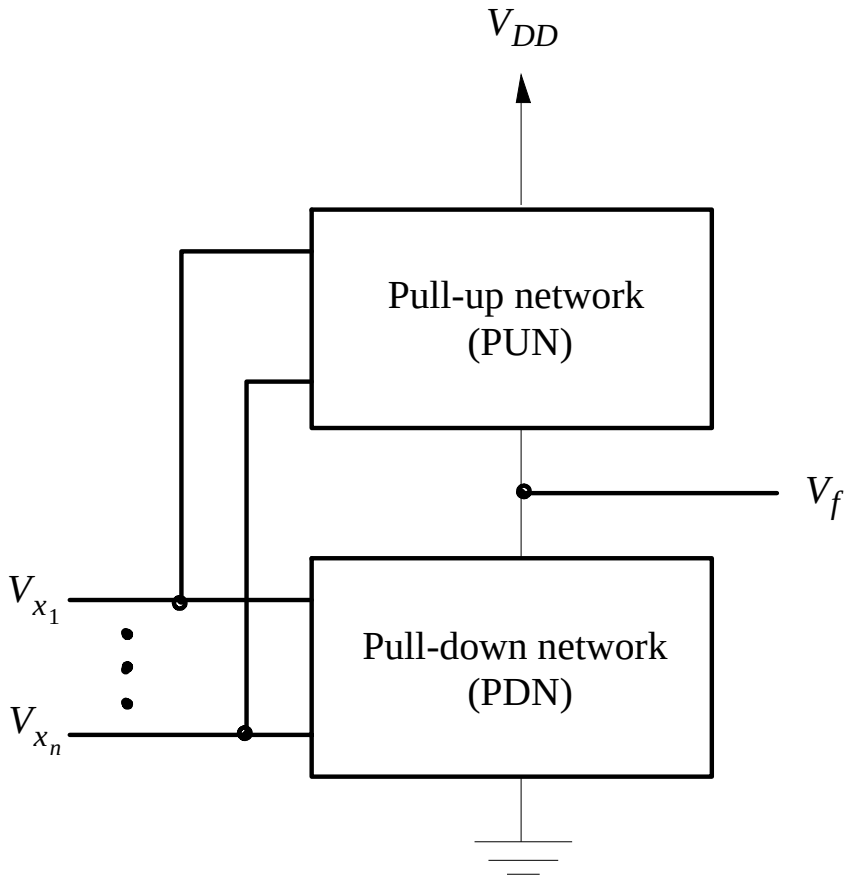
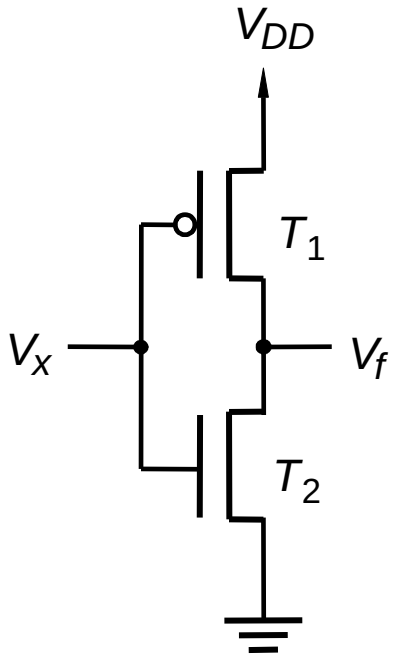


Figure 3.11. Structure of a CMOS circuit.

Implementação com CMOS

- PDN e PUN têm a mesma quantidade de transistores, arranjados de modo que haja uma dualidade entre as redes
- Sempre que PDN tiver transistores em série, a PUN terá transistores em paralelo e vice-versa
- Sob condições estáticas não há corrente fluindo entre o V_{DD} e o Gnd

Porta NOT com CMOS



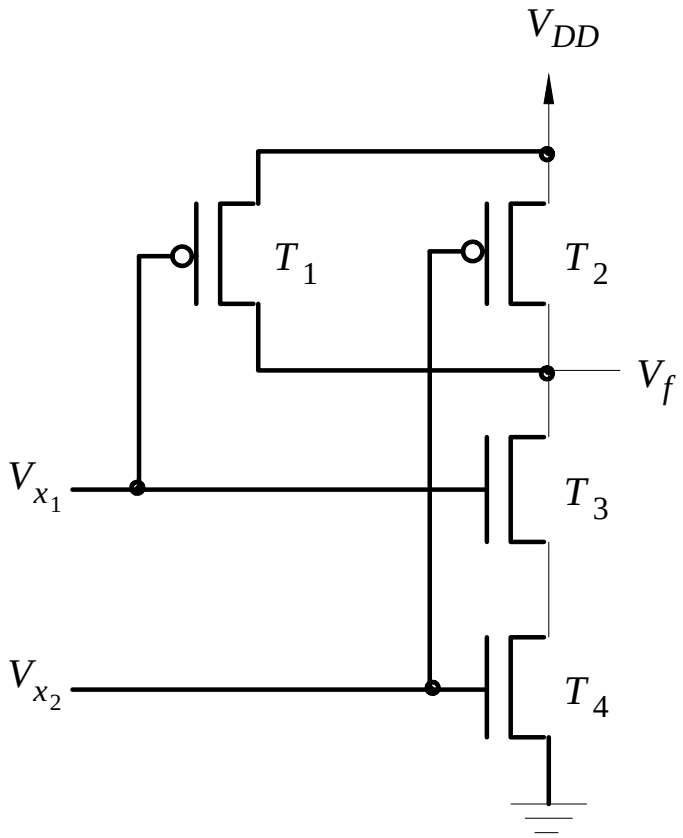
Qual a vantagem de se utilizar CMOS?

x	T_1	T_2	f
0	on	off	1
1	off	on	0

(a) Circuit

(b) Truth table and transistor states

Figure 3.12. CMOS realization of a NOT gate.

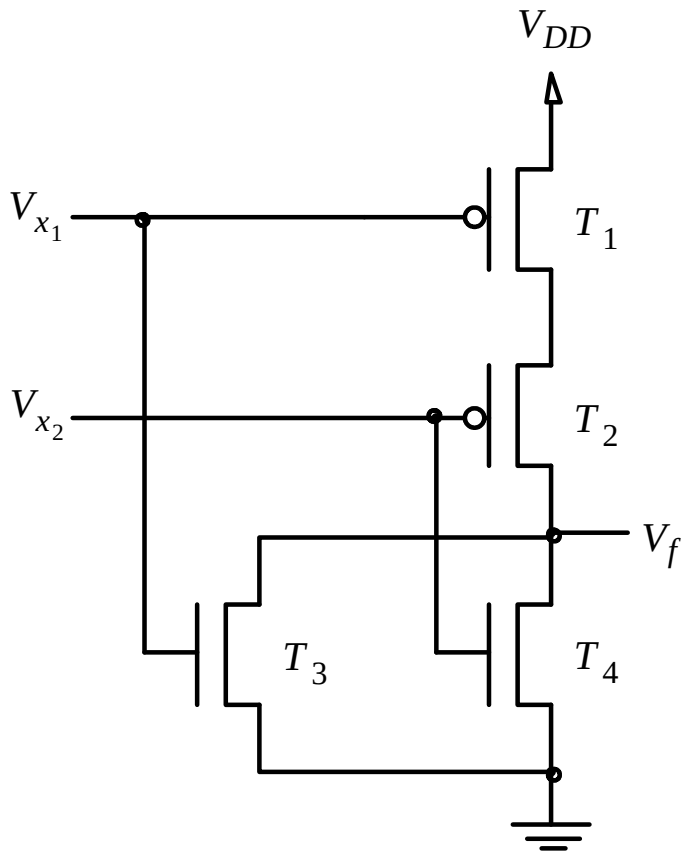


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

Figure 3.13. CMOS realization of a NAND gate.



(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

Figure 3.14. CMOS realization of a NOR gate.

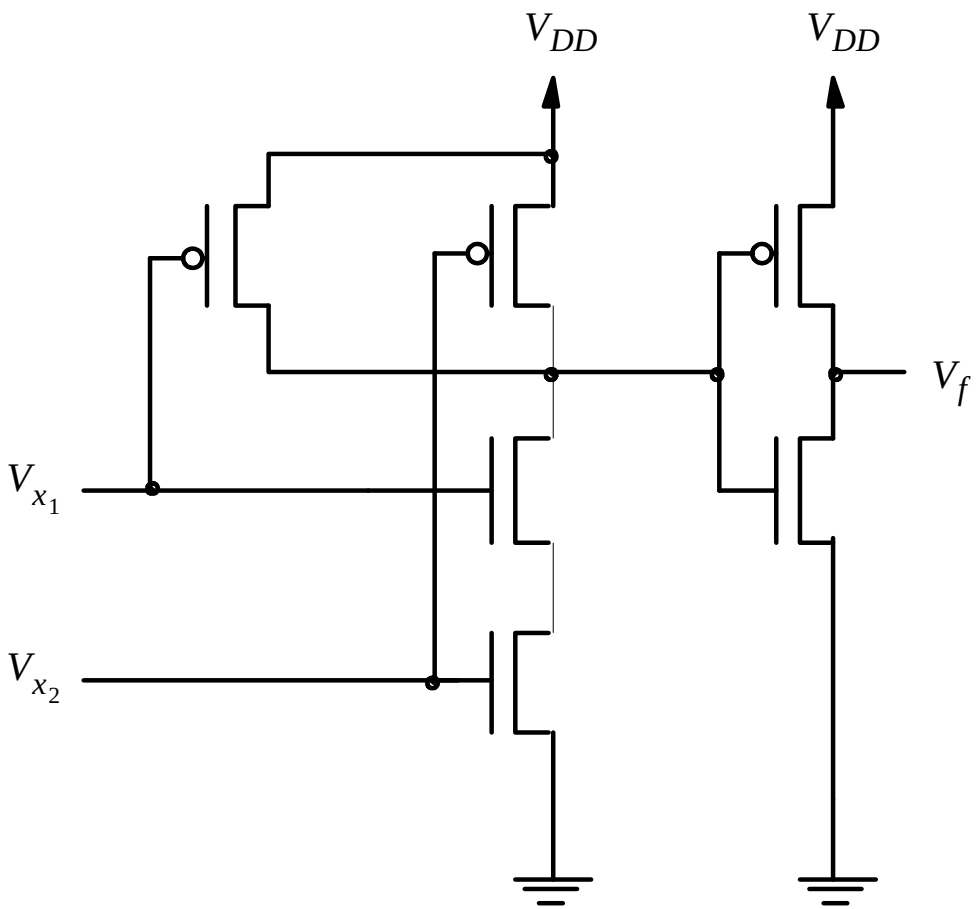


Figure 3.15. CMOS realization of an AND gate.

$$f = \overline{x_1} + \overline{x_2} \cdot \overline{x_3}$$

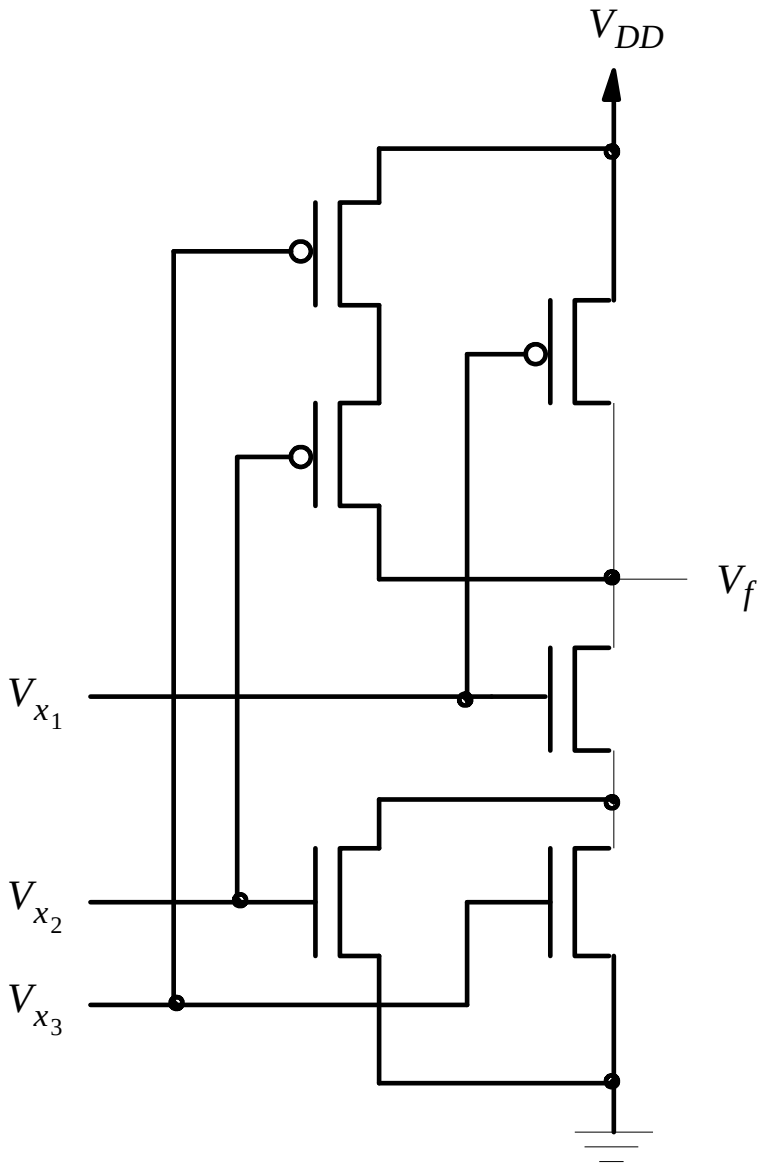
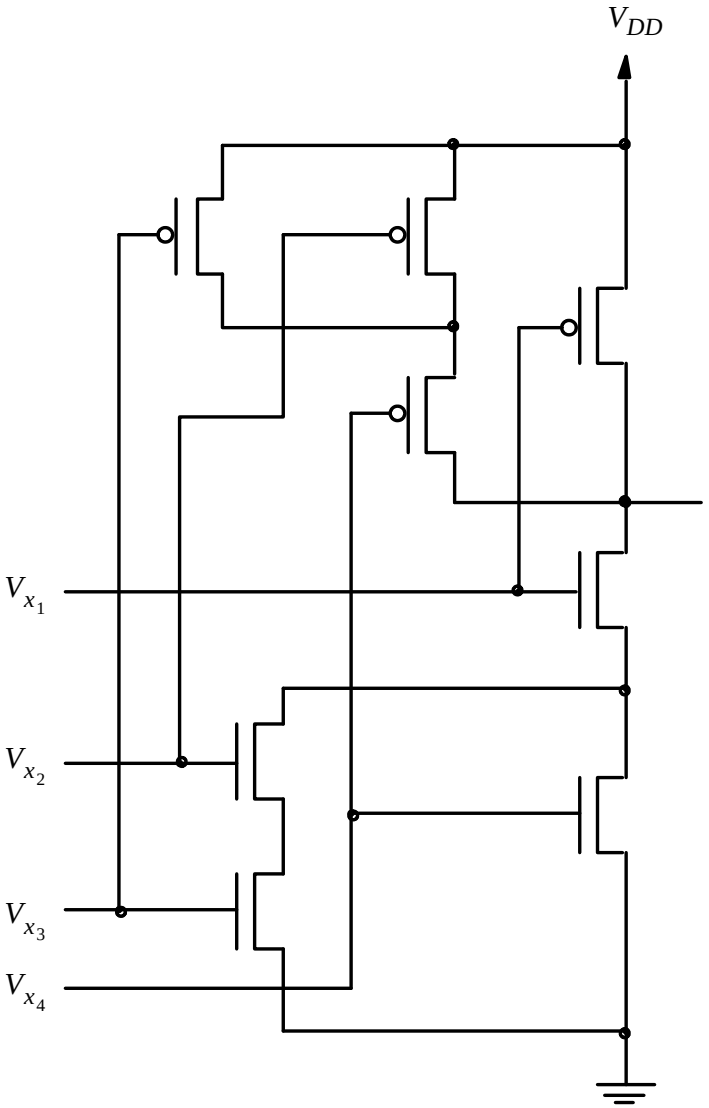


Figure 3.16. The circuit for Example 3.1.

- Construa o circuito CMOS para a seguinte função

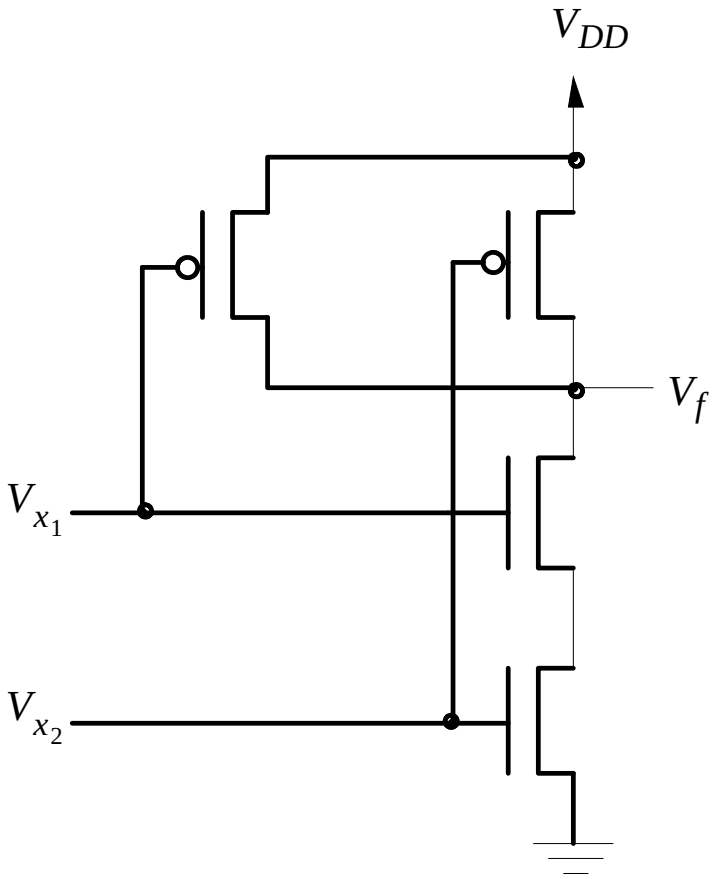
$$f = \overline{x}_1 + (\overline{x}_2 + \overline{x}_3)\,\overline{x}_4$$

Resposta do exercício anterior



Note que é possível construir circuitos relativamente complexos usando a combinação de transistores em paralelo e em série, sem necessariamente implementar cada conexão paralela ou serial como portas AND ou OR completas

Figure 3.17. The circuit for Example 3.2.



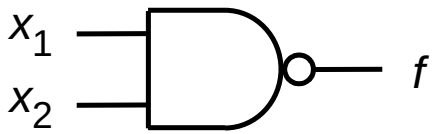
(a) Circuit

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

(b) Voltage levels

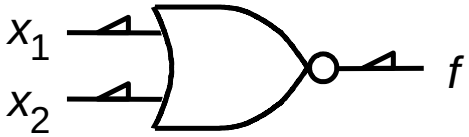
Figure 3.18. Voltage levels in the circuit in Figure 3.13.

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0



(a) Positive logic truth table and gate symbol

x_1	x_2	f
1	1	0
1	0	0
0	1	0
0	0	1



(b) Negative logic truth table and gate symbol

Figure 3.19. Interpretation of the circuit in Figure 3.18.

V_{x_1}	V_{x_2}	V_f
L	L	L
L	H	L
H	L	L
H	H	H

(a) Voltage levels

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

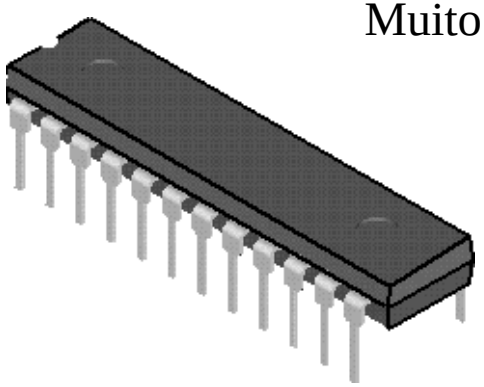
(b) Positive logic

x_1	x_2	f
1	1	1
1	0	1
0	1	1
0	0	0

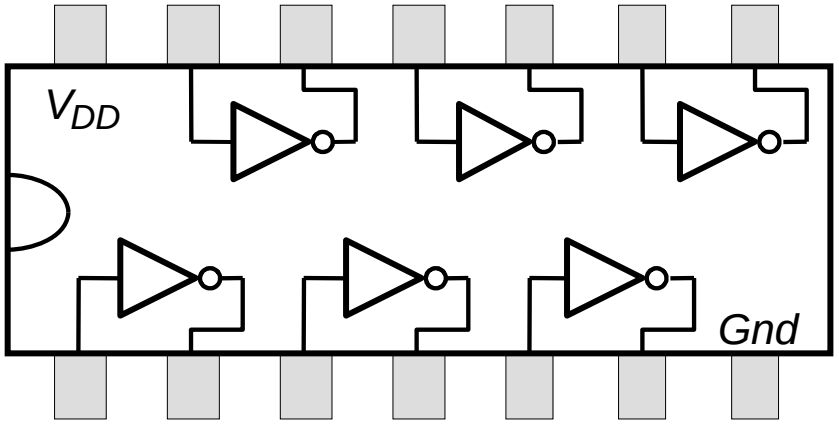
(c) Negative logic

Figure 3.20. Interpretation of the circuit in Figure 3.15.

Muito usado até meados de 1980



(a) Dual-inline package (DIP)



(b) Structure of 7404 chip

Figure 3.21. A 7400-series chip.

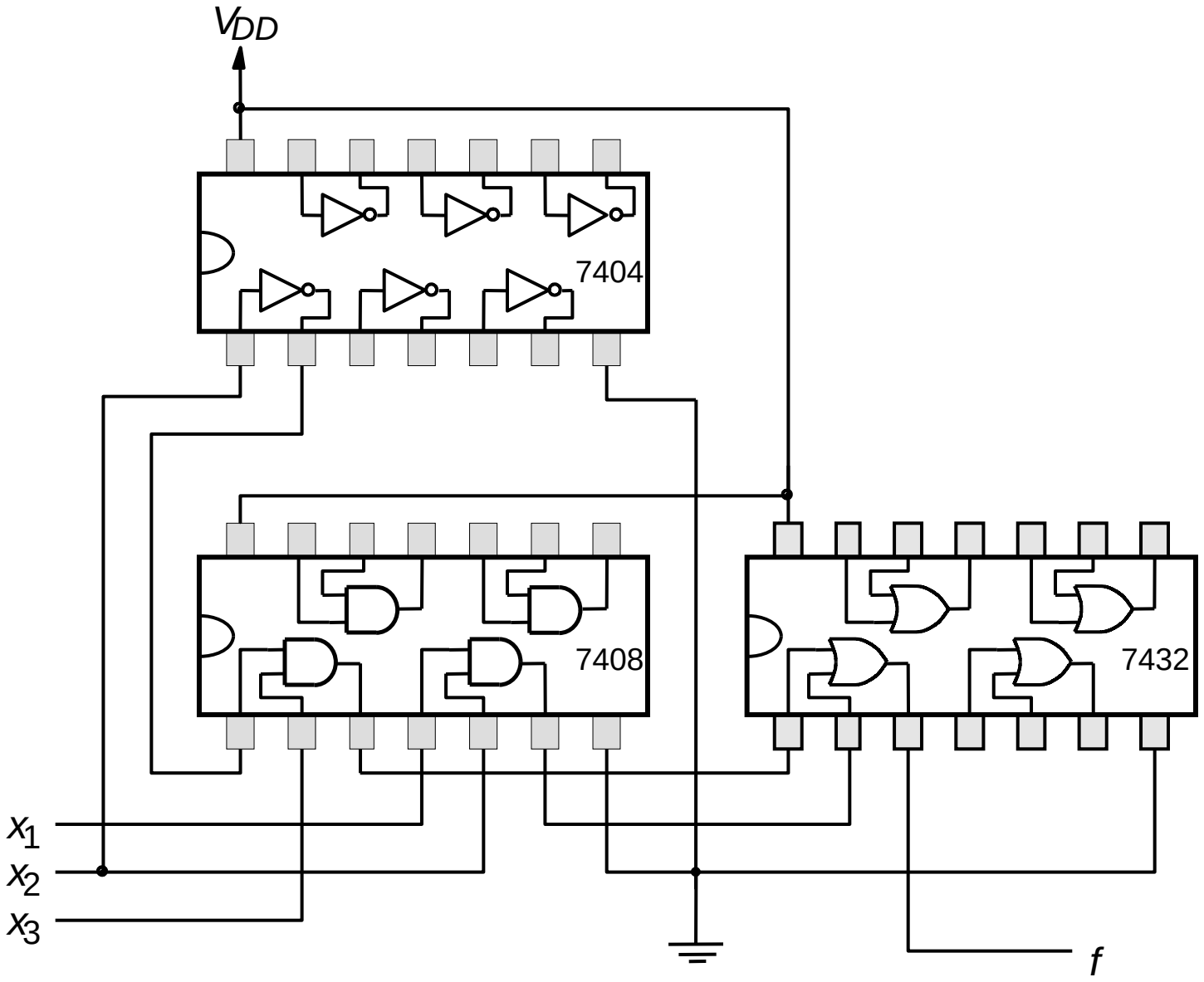


Figure 3.22. An implementation of $f = x_1x_2 + \bar{x}_2x_3$.

Buffer *tri-state*

Buffers são normalmente utilizados para aumentar a velocidade dos circuitos

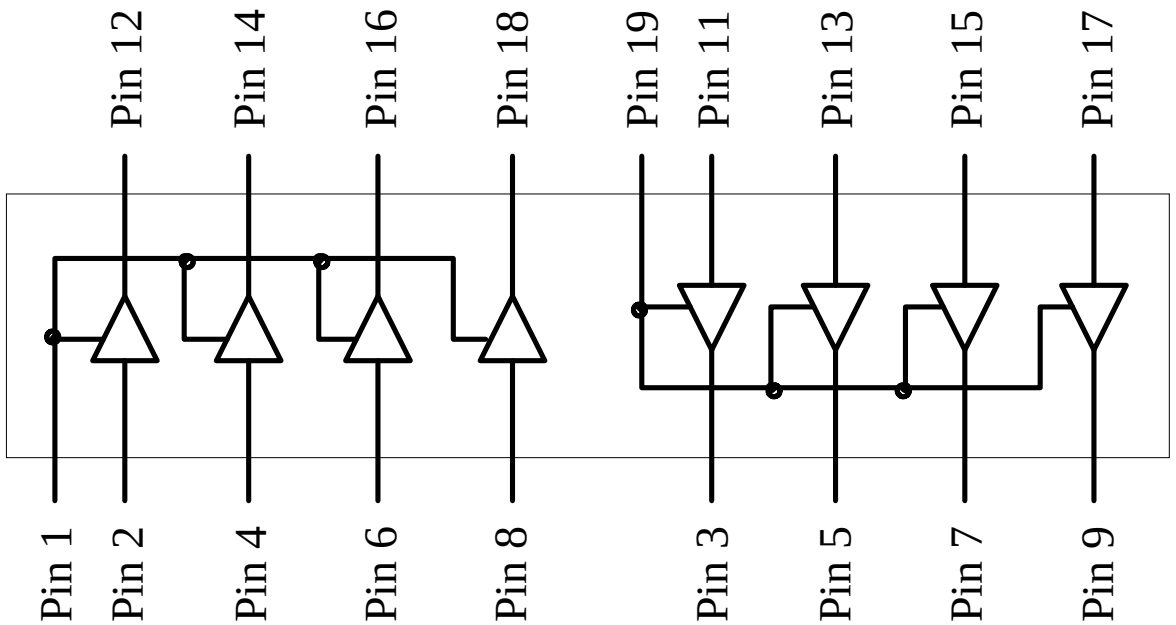


Figure 3.23. The 74244 buffer chip.

Avanço dos CIs

- SSI (Small-Scale Integration)
- MSI (Medium-Scale Integration)
  - Entre 10 e 100 portas lógicas
- LSI (Large-Scale Integration)
- VLSI (Very Large Scale Integration)
  - Milhões/Bilhões de transistores
  - Essa é a tecnologia mais utilizada atualmente

Processos usados pela Intel

- Intel® Itanium® com 2 bilhões de transistores

Process Name	P1264	P1266	P1268	P1270	P1272
Lithography	65nm	45nm	32nm	22nm	16nm
1st Production	2005	2007	2009	2011	2013