68,416 LEs FPGA

32M Byte X2 SDRAM

2M Byte SSRAM

8M Byte FLASH

X2 TV Decoder

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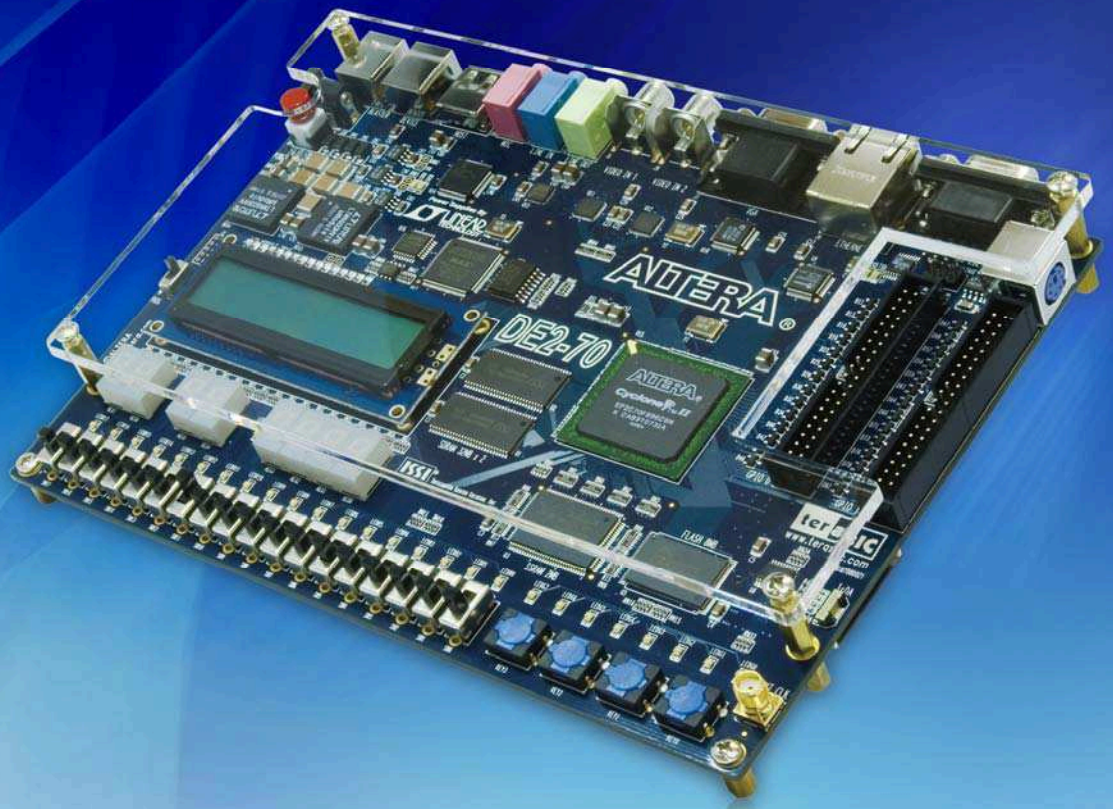

ALTERA®

Learning through Innovation

DE2-70

Development and Education Board

User Manual

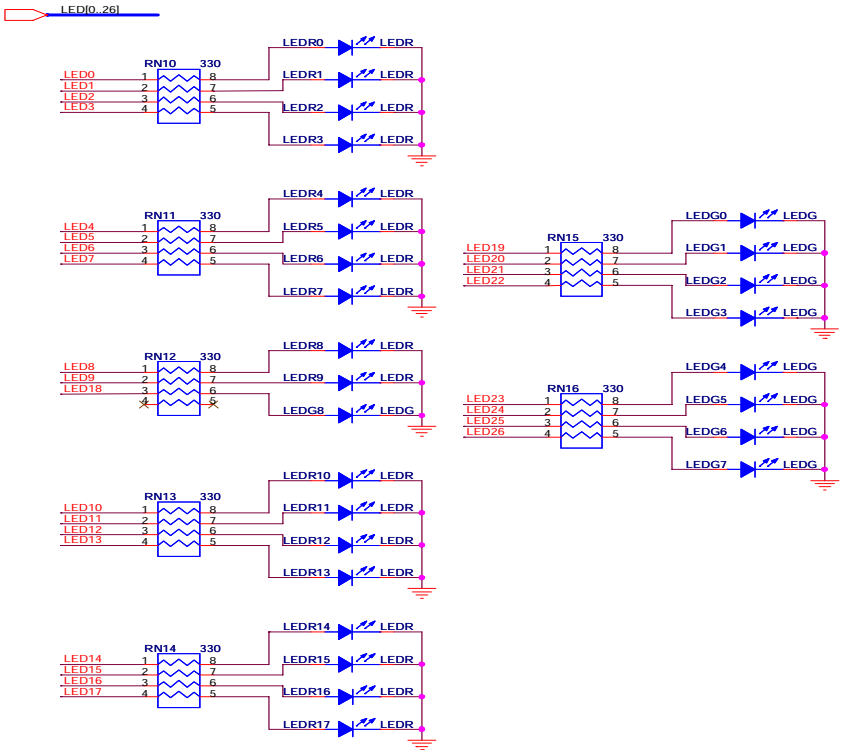

Figure 5.5. Schematic diagram of the LEDs.

Signal Name	FPGA Pin No.	Description
SW[0]	PIN_AA23	Toggle Switch[0]
SW[1]	PIN_AB26	Toggle Switch[1]
SW[2]	PIN_AB25	Toggle Switch[2]
SW[3]	PIN_AC27	Toggle Switch[3]
SW[4]	PIN_AC26	Toggle Switch[4]
SW[5]	PIN_AC24	Toggle Switch[5]
SW[6]	PIN_AC23	Toggle Switch[6]
SW[7]	PIN_AD25	Toggle Switch[7]
SW[8]	PIN_AD24	Toggle Switch[8]
SW[9]	PIN_AE27	Toggle Switch[9]
SW[10]	PIN_W5	Toggle Switch[10]
SW[11]	PIN_V10	Toggle Switch[11]
SW[12]	PIN_U9	Toggle Switch[12]
SW[13]	PIN_T9	Toggle Switch[13]
SW[14]	PIN_L5	Toggle Switch[14]
SW[15]	PIN_L4	Toggle Switch[15]

SW[16]	PIN_L7	Toggle Switch[16]
SW[17]	PIN_L8	Toggle Switch[17]

Table 5.1. Pin assignments for the toggle switches.

Signal Name	FPGA Pin No.	Description
KEY[0]	PIN_T29	Pushbutton[0]
KEY[1]	PIN_T28	Pushbutton[1]
KEY[2]	PIN_U30	Pushbutton[2]
KEY[3]	PIN_U29	Pushbutton[3]

Table 5.2. Pin assignments for the pushbutton switches.

Signal Name	FPGA Pin No.	Description
LEDR[0]	PIN_AJ6	LED Red[0]
LEDR[1]	PIN_ AK5	LED Red[1]
LEDR[2]	PIN_AJ5	LED Red[2]
LEDR[3]	PIN_AJ4	LED Red[3]
LEDR[4]	PIN_AK3	LED Red[4]
LEDR[5]	PIN_AH4	LED Red[5]
LEDR[6]	PIN_AJ3	LED Red[6]
LEDR[7]	PIN_AJ2	LED Red[7]
LEDR[8]	PIN_AH3	LED Red[8]
LEDR[9]	PIN_AD14	LED Red[9]
LEDR[10]	PIN_AC13	LED Red[10]
LEDR[11]	PIN_AB13	LED Red[11]
LEDR[12]	PIN_AC12	LED Red[12]
LEDR[13]	PIN_AB12	LED Red[13]
LEDR[14]	PIN_AC11	LED Red[14]
LEDR[15]	PIN_AD9	LED Red[15]
LEDR[16]	PIN_AD8	LED Red[16]
LEDR[17]	PIN_AJ7	LED Red[17]
LEDG[0]	PIN_W27	LED Green[0]
LEDG[1]	PIN_ W25	LED Green[1]
LEDG[2]	PIN_ W23	LED Green[2]
LEDG[3]	PIN_ Y27	LED Green[3]
LEDG[4]	PIN_ Y24	LED Green[4]
LEDG[5]	PIN_ Y23	LED Green[5]
LEDG[6]	PIN_ AA27	LED Green[6]

LEDG[7]	PIN_ AA24	LED Green[7]
LEDG[8]	PIN_ AC14	LED Green[8]

Table 5.3. Pin assignments for the LEDs.

5.3 Using the 7-segment Displays

The DE2-70 Board has eight 7-segment displays. These displays are arranged into two pairs and a group of four, with the intent of displaying numbers of various sizes. As indicated in the schematic in Figure 5.6, the seven segments are connected to pins on the Cyclone II FPGA. Applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off.

Each segment in a display is identified by an index from 0 to 6, with the positions given in Figure 5.7. In addition, the decimal point is identified as DP. Table 5.4 shows the assignments of FPGA pins to the 7-segment displays.

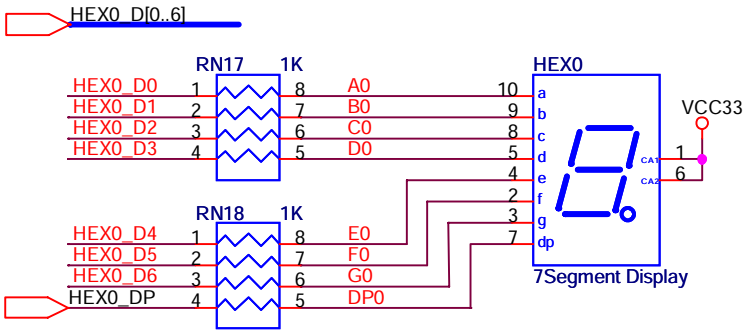

Figure 5.6. Schematic diagram of the 7-segment displays.

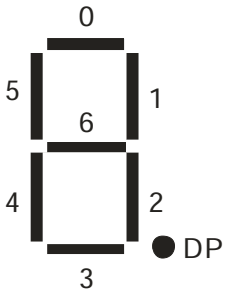

Figure 5.7. Position and index of each segment in a 7-segment display.

Signal Name	FPGA Pin No.	Description
HEX0_D[0]	PIN_AE8	Seven Segment Digit 0[0]
HEX0_D[1]	PIN_AF9	Seven Segment Digit 0[1]
HEX0_D[2]	PIN_AH9	Seven Segment Digit 0[2]

HEX0_D[3]	PIN_AD10	Seven Segment Digit 0[3]
HEX0_D[4]	PIN_AF10	Seven Segment Digit 0[4]
HEX0_D[5]	PIN_AD11	Seven Segment Digit 0[5]
HEX0_D[6]	PIN_AD12	Seven Segment Digit 0[6]
HEX0_DP	PIN_AF12	Seven Segment Decimal Point 0
HEX1_D[0]	PIN_ AG13	Seven Segment Digit 1[0]
HEX1_D[1]	PIN_ AE16	Seven Segment Digit 1[1]
HEX1_D[2]	PIN_ AF16	Seven Segment Digit 1[2]
HEX1_D[3]	PIN_AG16	Seven Segment Digit 1[3]
HEX1_D[4]	PIN_AE17	Seven Segment Digit 1[4]
HEX1_D[5]	PIN_AF17	Seven Segment Digit 1[5]
HEX1_D[6]	PIN_AD17	Seven Segment Digit 1[6]
HEX1_DP	PIN_ AC17	Seven Segment Decimal Point 1
HEX2_D[0]	PIN_AE7	Seven Segment Digit 2[0]
HEX2_D[1]	PIN_AF7	Seven Segment Digit 2[1]
HEX2_D[2]	PIN_AH5	Seven Segment Digit 2[2]
HEX2_D[3]	PIN_AG4	Seven Segment Digit 2[3]
HEX2_D[4]	PIN_AB18	Seven Segment Digit 2[4]
HEX2_D[5]	PIN_AB19	Seven Segment Digit 2[5]
HEX2_D[6]	PIN_AE19	Seven Segment Digit 2[6]
HEX2_DP	PIN_AC19	Seven Segment Decimal Point 2
HEX3_D[0]	PIN_P6	Seven Segment Digit 3[0]
HEX3_D[1]	PIN_P4	Seven Segment Digit 3[1]
HEX3_D[2]	PIN_N10	Seven Segment Digit 3[2]
HEX3_D[3]	PIN_N7	Seven Segment Digit 3[3]
HEX3_D[4]	PIN_M8	Seven Segment Digit 3[4]
HEX3_D[5]	PIN_M7	Seven Segment Digit 3[5]
HEX3_D[6]	PIN_M6	Seven Segment Digit 3[6]
HEX3_DP	PIN_M4	Seven Segment Decimal Point 3
HEX4_D[0]	PIN_P1	Seven Segment Digit 4[0]
HEX4_D[1]	PIN_P2	Seven Segment Digit 4[1]
HEX4_D[2]	PIN_P3	Seven Segment Digit 4[2]
HEX4_D[3]	PIN_N2	Seven Segment Digit 4[3]
HEX4_D[4]	PIN_N3	Seven Segment Digit 4[4]
HEX4_D[5]	PIN_M1	Seven Segment Digit 4[5]
HEX4_D[6]	PIN_M2	Seven Segment Digit 4[6]
HEX4_DP	PIN_L6	Seven Segment Decimal Point 4

HEX5_D[0]	PIN_M3	Seven Segment Digit 5[0]
HEX5_D[1]	PIN_L1	Seven Segment Digit 5[1]
HEX5_D[2]	PIN_L2	Seven Segment Digit 5[2]
HEX5_D[3]	PIN_L3	Seven Segment Digit 5[3]
HEX5_D[4]	PIN_K1	Seven Segment Digit 5[4]
HEX5_D[5]	PIN_K4	Seven Segment Digit 5[5]
HEX5_D[6]	PIN_K5	Seven Segment Digit 5[6]
HEX5_DP	PIN_K6	Seven Segment Decimal Point 5
HEX6_D[0]	PIN_H6	Seven Segment Digit 6[0]
HEX6_D[1]	PIN_H4	Seven Segment Digit 6[1]
HEX6_D[2]	PIN_H7	Seven Segment Digit 6[2]
HEX6_D[3]	PIN_H8	Seven Segment Digit 6[3]
HEX6_D[4]	PIN_G4	Seven Segment Digit 6[4]
HEX6_D[5]	PIN_F4	Seven Segment Digit 6[5]
HEX6_D[6]	PIN_E4	Seven Segment Digit 6[6]
HEX6_DP	PIN_K2	Seven Segment Decimal Point 6
HEX7_D[0]	PIN_K3	Seven Segment Digit 7[0]
HEX7_D[1]	PIN_J1	Seven Segment Digit 7[1]
HEX7_D[2]	PIN_J2	Seven Segment Digit 7[2]
HEX7_D[3]	PIN_H1	Seven Segment Digit 7[3]
HEX7_D[4]	PIN_H2	Seven Segment Digit 7[4]
HEX7_D[5]	PIN_H3	Seven Segment Digit 7[5]
HEX7_D[6]	PIN_G1	Seven Segment Digit 7[6]
HEX7_DP	PIN_G2	Seven Segment Decimal Point 7

Table 5.4. Pin assignments for the 7-segment displays.

5.4 Clock Circuitry

The DE2-70 board includes two oscillators that produce 28.86 MHz and 50 MHz clock signals. Both two clock signals are connected to the FPGA that are used for clocking the user logic. Also, the 28.86 MHz oscillator is used to drive the two TV decoders. The board also includes an SMA connector which can be used to connect an external clock source to the board. In addition, all these clock inputs are connected to the phase lock loops (PLL) clock input pin of the FPGA allowed users can use these clocks as a source clock for the PLL circuit.

The clock distribution on the DE2-70 board is shown in Figure 5.8. The associated pin assignments for clock inputs to FPGA I/O pins are listed in Table 5.5.

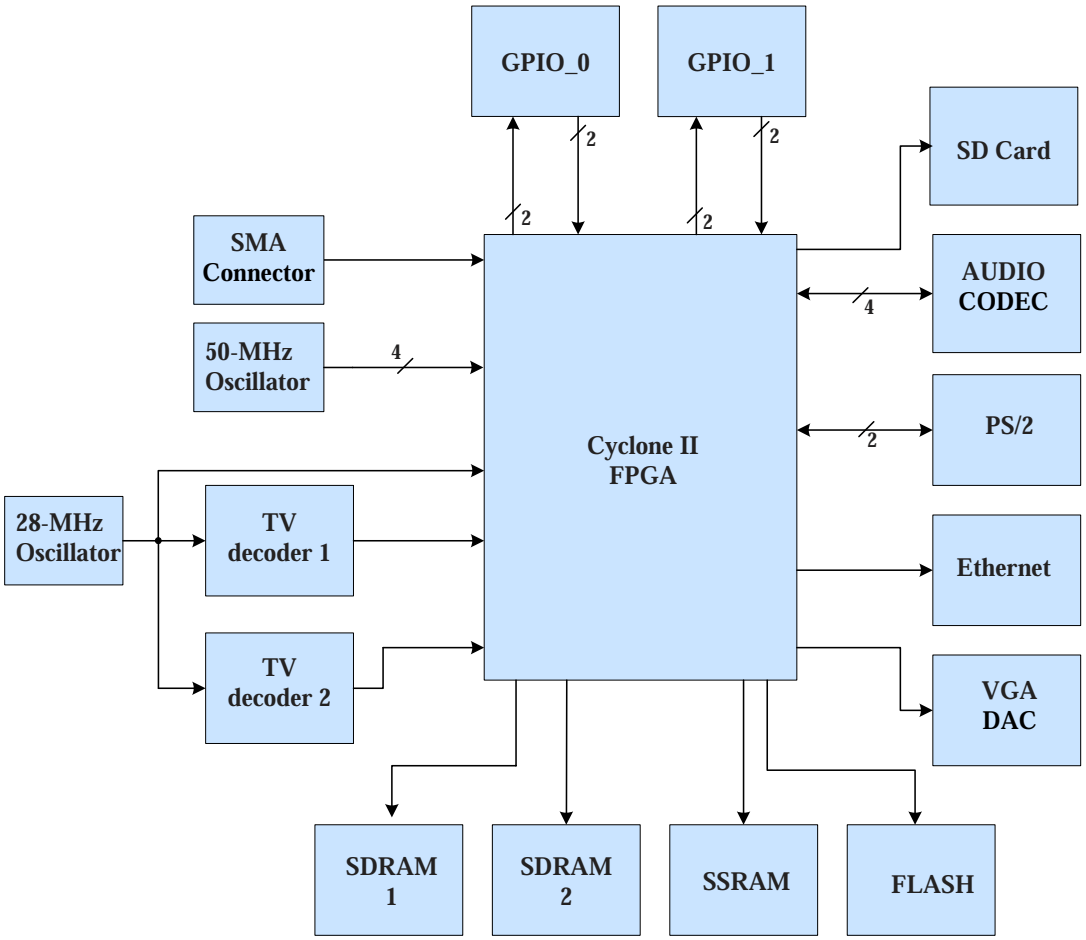

Figure 5.8. Block diagram of the clock distribution.

Signal Name	FPGA Pin No.	Description
CLK_28	PIN_E16	28 MHz clock input
CLK_50	PIN_AD15	50 MHz clock input
CLK_50_2	PIN_D16	50 MHz clock input
CLK_50_3	PIN_R28	50 MHz clock input
CLK_50_4	PIN_R3	50 MHz clock input
EXT_CLOCK	PIN_R29	External (SMA) clock input

Table 5.5. Pin assignments for the clock inputs.