

**USP - ICMC - SSC  
SSC 0111 (Lab ELD I) - 2o. Semestre 2011**

**Disciplina de  
Laboratório de Elementos de Lógica Digital I  
SSC-0111**

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**Wiki ICMC: [http://wiki.icmc.usp.br/index.php/SSC-111\(fosorio\)](http://wiki.icmc.usp.br/index.php/SSC-111(fosorio))**

**Aula 04 – Circuitos Lógicos e Simulação**

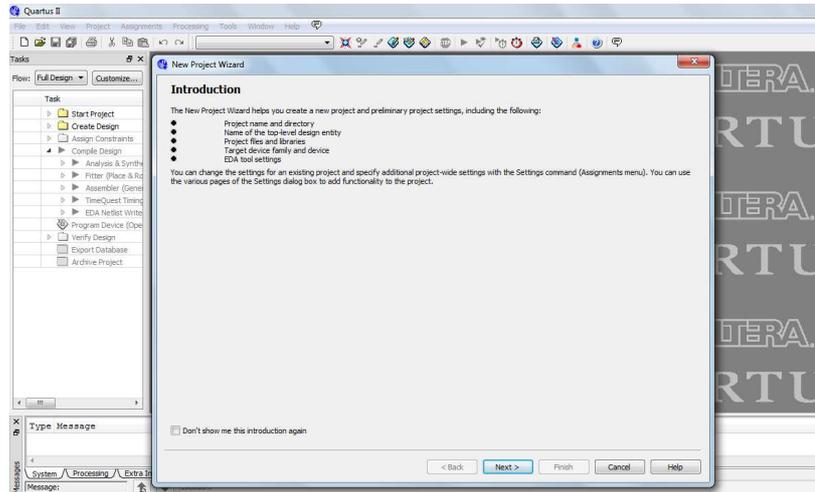
**Agenda:**

- 1. Quartus II – Editando Circuitos**  
**Editor de Diagramas Esquemáticos**
- 2. Quartus II – Simulação de Circuitos**  
**Waveform Editor / Simulador**
- 3. Projeto de Circuito em FPGA**  
**Xor , Half-Adder , Full-Adder**  
**Somador: Implementação e Simulação**

## 1. Quartus II – Edição de Circuitos

### Editor de Diagramas Esquemáticos

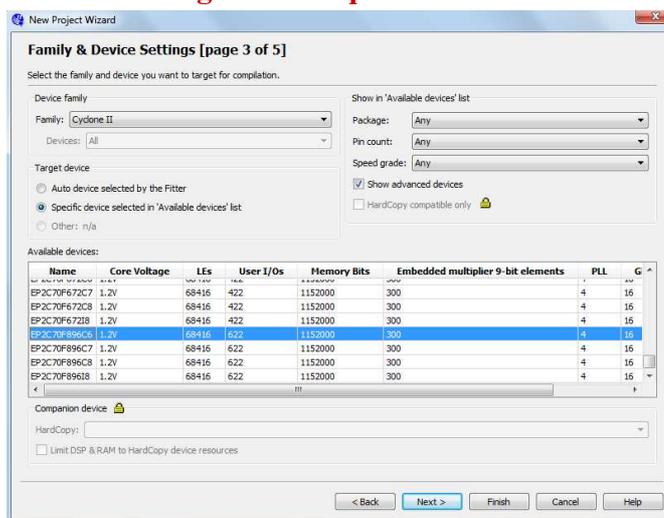
New Project Wizard



## 1. Quartus II – Edição de Circuitos

### Editor de Diagramas Esquemáticos

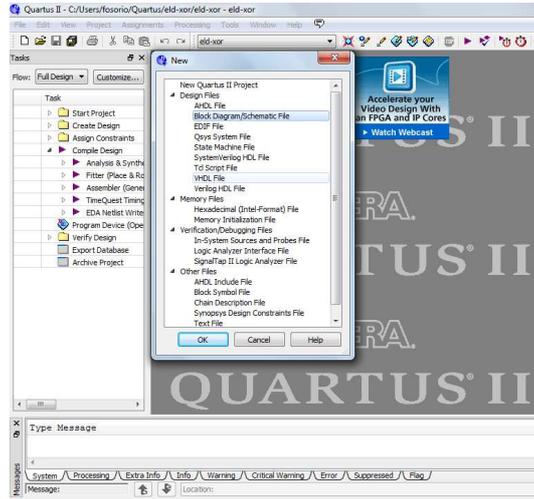
New Project Wizard  
 DE2-70  
 EP2C70F896C6



## 1. Quartus II – Edição de Circuitos

### Editor de Diagramas Esquemáticos

New  
Block Diagram  
Schematic File



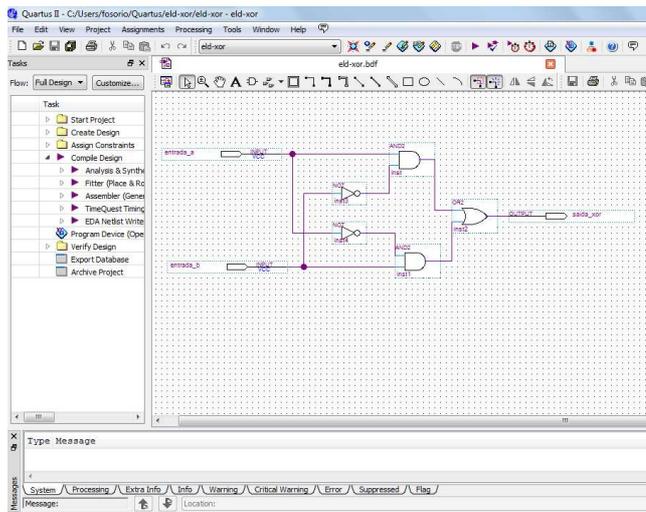
## 1. Quartus II – Edição de Circuitos

### Editor de Diagramas Esquemáticos

New  
Block Diagram  
Schematic File

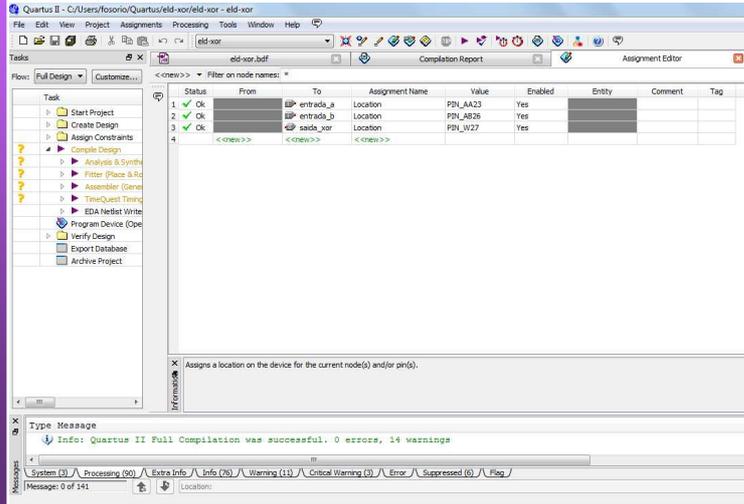
QPF:  
Quartus Project File

BDF:  
Block Diagram File



# 1. Quartus II – Edição de Circuitos

## Editor de Diagramas Esquemáticos



New  
Block Diagram  
Schematic File

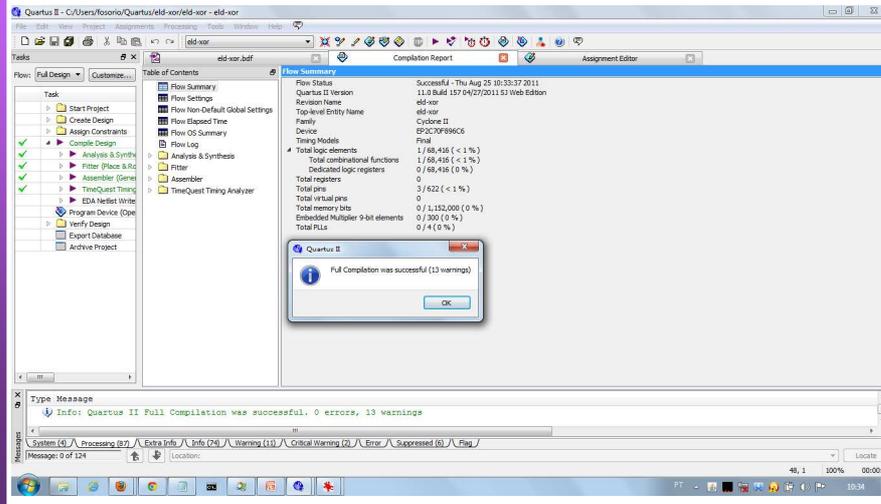
QPF:  
Quartus Project File

BDF:  
Block Diagram File

...  
Compile  
Assignment Editor  
(pinagem)

# 1. Quartus II – Edição de Circuitos

## Editor de Diagramas Esquemáticos



## 2. Quartus II – Simulação de Circuitos

### Simulação de Circuitos: Functional / Timing => Q11 / Q9

QUARTUS II: <http://www.altera.com/education/univ/software/qsim/unv-qsim.html>

**ALTERA** **QSIM – Quartus II** [Download Center](#) [Literature](#) [Sign in/register myAltera Account](#)

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**Educational Materials**  
 Dev. & Education Boards  
 Software Tools  
 Quartus II  
 Quartus II Simulator  
 Nios II  
 Altera Monitor Program  
 ModelSim-Altera  
 University Program  
 Installer  
 DSP Builder  
 Digital Logic  
 Computer Organization  
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**Events**  
 Conferences  
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 Overview  
 QUP

**Quartus II Simulator Tools for Education**  
[Home](#) > [Training](#) > [University Program](#) > [Software Tools](#) > [Quartus II Simulator](#)

The Quartus® II Simulator tools consist of two programs: QSim and the Waveform Editor. QSim is a graphical user interface (GUI) that is used to run simulations and launch the Waveform Editor. Also, QSim is used to set whether the simulation should be a functional or timing simulation. The Vector Waveform Editor is used to draw the test input signals for the simulation and select which signal should be shown in the simulation results.

The following table shows the available tutorial for these tools and the program used to install these tools. This installer is to be used in conjunction with the Quartus II software versions 11.0 and 10.1 only.

**Filter Materials**  
 Choose HDL:  Choose Quartus II Version:

**Table 1. Simulation Tools for Quartus II 11.0**

Title	Downloads
Tutorials	
Introduction to Simulation	<a href="#">PDF</a>
Tools	
University Program Installer	<a href="#">EXE</a>

Rate This Page

## 2. Quartus II – Simulação de Circuitos

### Simulação de Circuitos: Functional / Timing => Q11 / Q9

**Qsim**  
 File Assign Processing Help

**Console Window**

```
>> To get started, open an existing Quartus II project by selecting "File > Open Project..."
>> To produce an input waveform file, select "File > New Simulation Input".
>> In the displayed window, create the desired input waveforms. Give it a suitable name and save it.
>>
>> To specify a setting for simulation, select "Assign > Simulation Settings".
>> In the pop-up dialog box, choose a specific VWF file and specify either functional or timing simulation.
>> Run the simulation by selecting "Processing > Start Simulation".
>>
>> Warning: If you recompile your Quartus II project with new changes, the Node Finder Files may be invalid.
>> To prevent invalid nodes from showing up in the Node Finder, regenerate the Node Finder files
>> by selecting "Processing > Generate Node Finder Files", after you recompiled your project.
```

**Qsim - eld-xor**  
 File Assign Processing Help

- Open Project... **Ctrl+O**
- Close Project
- New Simulation Input File**
- Open Simulation Input File
- Open Simulation Output File
- Exit **Alt+F4**

Open Project  
 New Simulation Input File  
 WAVEFORM EDITOR  
 VWF  
 Vector Waveform File

Version 11.0 Build 157 04/27/2011 SJ Web Edition



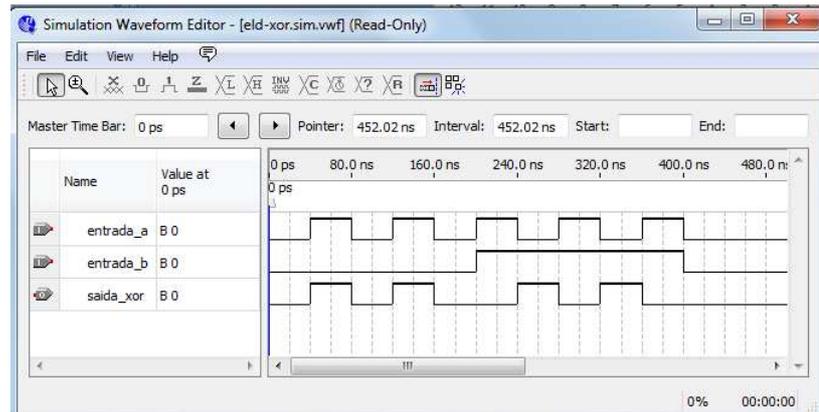
## 2. Quartus II – Simulação de Circuitos

### Simulação de Circuitos: Functional / Timing => Q11 / Q9

Open Project  
New Simulation Input File

WAVEFORM EDITOR  
VWF  
Vector Waveform File

RESULTADO DA SIMULAÇÃO



## 3. Projeto de Circuito em FPGA

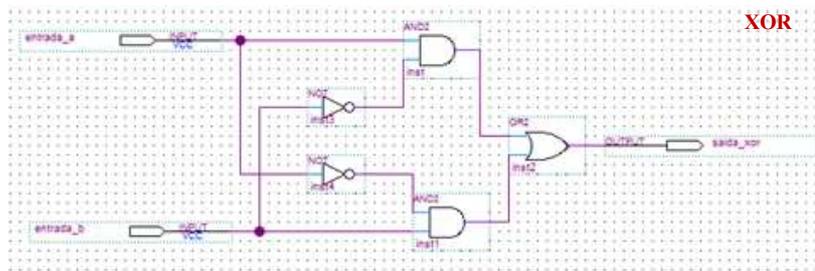
### Circuitos Lógicos

- XOR
- Half-Adder (meio somador)
- Full-Adder (somador completo)
- Somadores em Cascata

### 3. Projeto de Circuito em FPGA

#### Circuitos Lógicos

- XOR
- Half-Adder (meio somador)
- Full-Adder (somador completo)
- Somadores em Cascata



XOR

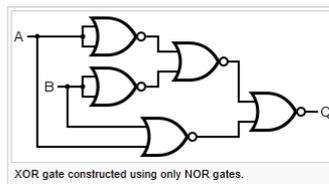
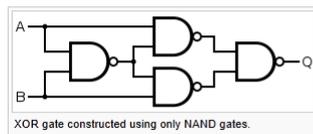
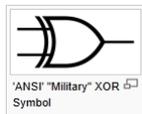
### 3. Projeto de Circuito em FPGA

#### Circuitos Lógicos

- XOR

INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

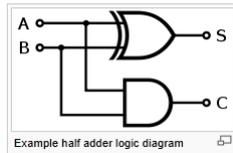
SOMA	A + B:
0 + 0	= 0
0 + 1	= 1
1 + 0	= 1
1 + 1	= 0 e vai_um



### 3. Projeto de Circuito em FPGA

#### Circuitos Lógicos

- Half-Adder



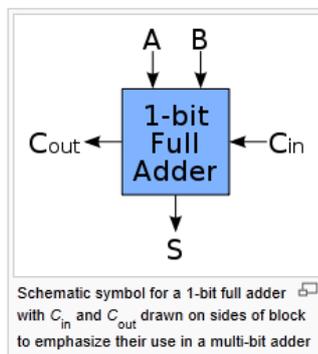
SOMA  
 $A + B = S \Rightarrow \text{XOR}$   
 VAI\_UM  
 $A + B = C \Rightarrow \text{AND}$

INPUT		OUTPUT		Vai_Um "Carry"
A	B	A XOR B		
0	0	0		0
0	1	1		0
1	0	1		0
1	1	0		1

### 3. Projeto de Circuito em FPGA

#### Circuitos Lógicos

- Full-Adder



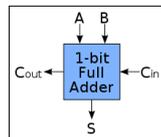
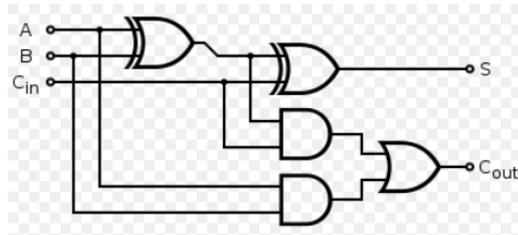
Inputs			Outputs	
A	B	$C_{in}$	$C_{out}$	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

### 3. Projeto de Circuito em FPGA

#### Circuitos Lógicos

- Full-Adder

Inputs			Outputs	
A	B	C <sub>in</sub>	C <sub>out</sub>	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

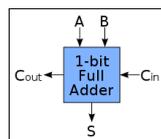
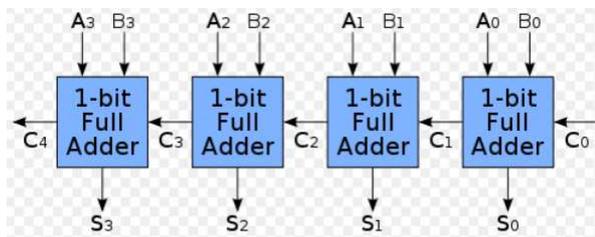


### 3. Projeto de Circuito em FPGA

#### Circuitos Lógicos

- Full-Adder em Cascata: Somador de 4 bits

Inputs			Outputs	
A	B	C <sub>in</sub>	C <sub>out</sub>	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1





**INFORMAÇÕES SOBRE A DISCIPLINA**

**USP - Universidade de São Paulo - São Carlos, SP**  
**ICMC - Instituto de Ciências Matemáticas e de Computação**  
**SSC - Departamento de Sistemas de Computação**

**LRM – Laboratório de Robótica Móvel**

**Web LRM: [Http://lrm.icmc.usp.br/](http://lrm.icmc.usp.br/)**

**Página pessoal: [Http://www.icmc.usp.br/~fosorio/](http://www.icmc.usp.br/~fosorio/)**

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**E-mail: [diogosoc \[at\] { icmc. usp. br }](mailto:diogosoc@icmc.usp.br) - Diogo Correa (PAE)**

**Disciplina de Laboratório de Elementos de Lógica Digital I [LELD1]**

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**Web Wiki: [Http://wiki.icmc.usp.br/index.php/SSC-111](http://wiki.icmc.usp.br/index.php/SSC-111)**

**> Programa, Material de Aulas, Critérios de Avaliação,**

**> Material de Apoio, Trabalhos Práticos**