USP - ICMC - SSC
SSC 0111 (Lab ELD I) - 2o. Semestre 2011

Disciplina de Laboratório de Elementos de Lógica Digital I SSC-0111

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Wiki ICMC: http://wiki.icmc.usp.br/index.php/SSC-111(fosorio)

Aula 04

Aula 04 – Circuitos Lógicos e Simulação

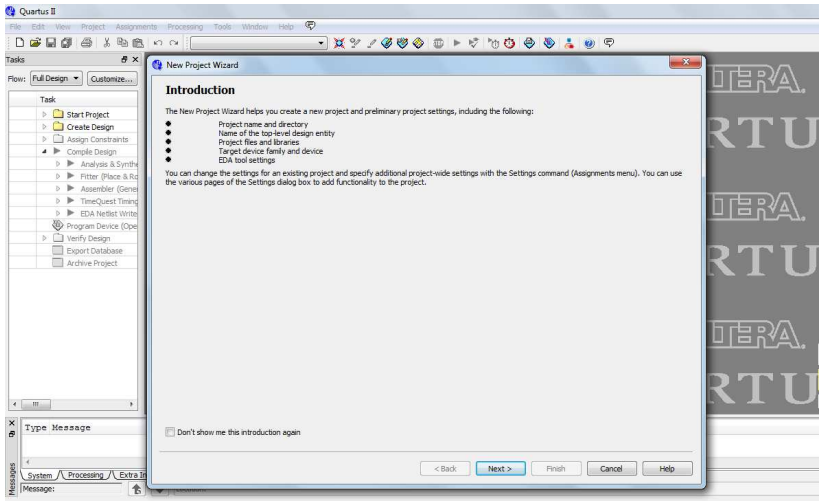
Agenda:

1. Quartus II – Editando Circuitos
   Editor de Diagramas Esquemáticos
2. Quartus II – Simulação de Circuitos
   Waveform Editor / Simulador
3. Projeto de Circuito em FPGA
   Xor , Half-Adder , Full-Adder
   Somador: Implementação e Simulação

1. Quartus II – Edição de Circuitos

Editor de Diagramas Esquemáticos

New Project Wizard



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1. Quartus II – Edição de Circuitos

Editor de Diagramas Esquemáticos

New Project Wizard
DE2-70
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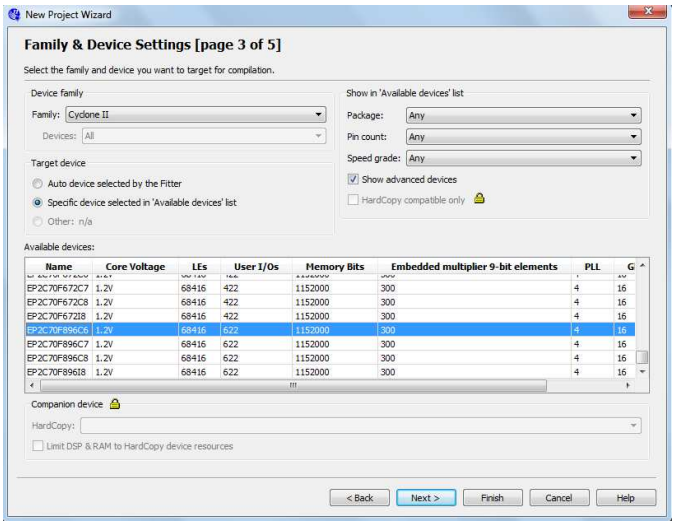
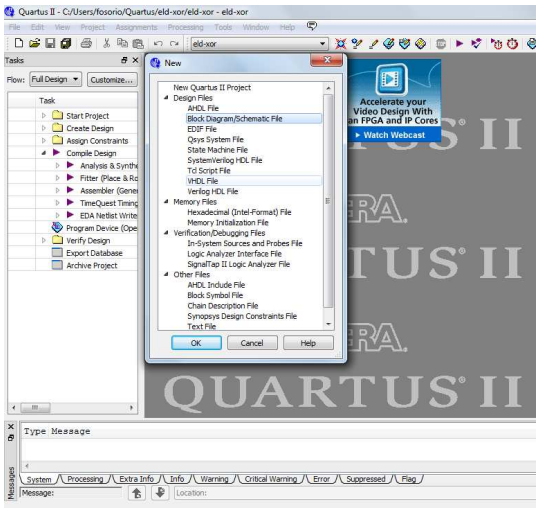


1. Quartus II – Edição de Circuitos

Editor de Diagramas Esquemáticos

New
Block Diagram
Schematic File



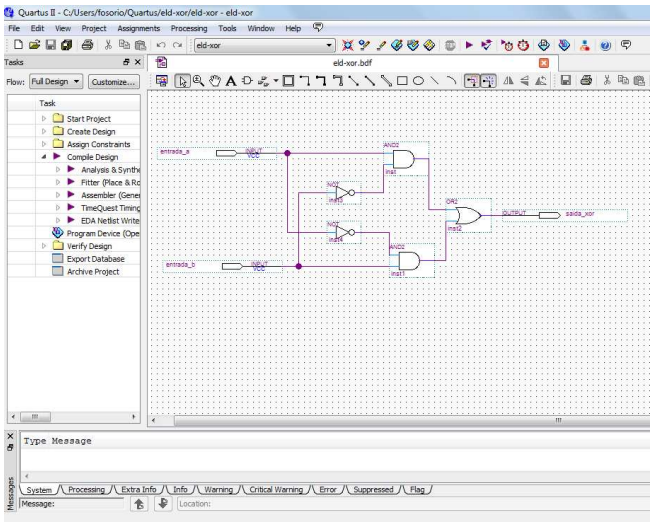
1. Quartus II – Edição de Circuitos

Editor de Diagramas Esquemáticos

New
Block Diagram
Schematic File

QPF:
Quartus Project File

BDF:
Block Diagram File



1. Quartus II – Edição de Circuitos

Editor de Diagramas Esquemáticos

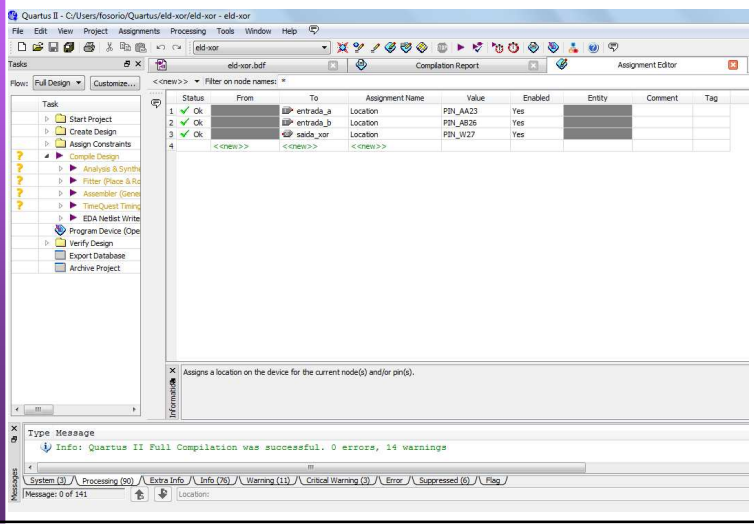
New
Block Diagram
Schematic File

QPF:
Quartus Project File

BDF:
Block Diagram File

...

Compile
Assignment Editor
(pinagem)



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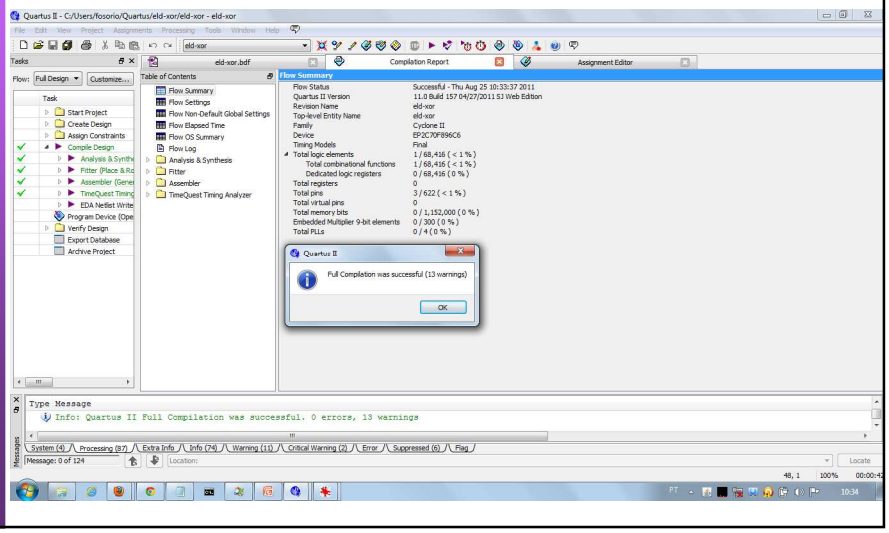
1. Quartus II – Edição de Circuitos

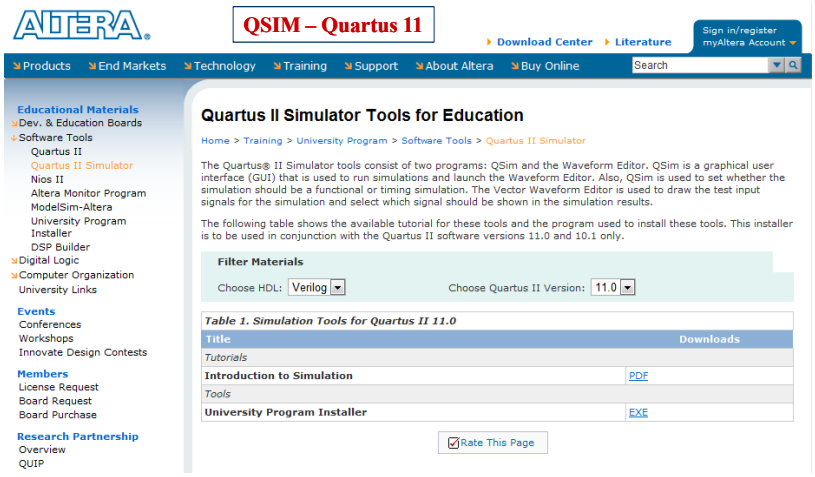
Editor de Diagramas Esquemáticos



2. Quartus II – Simulação de Circuitos

Simulação de Circuitos: Functional / Timing => Q11 / Q9

QUARTUS 11: http://www.altera.com/education/univ/software/qsim/unv-qsim.html



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2. Quartus II – Simulação de Circuitos

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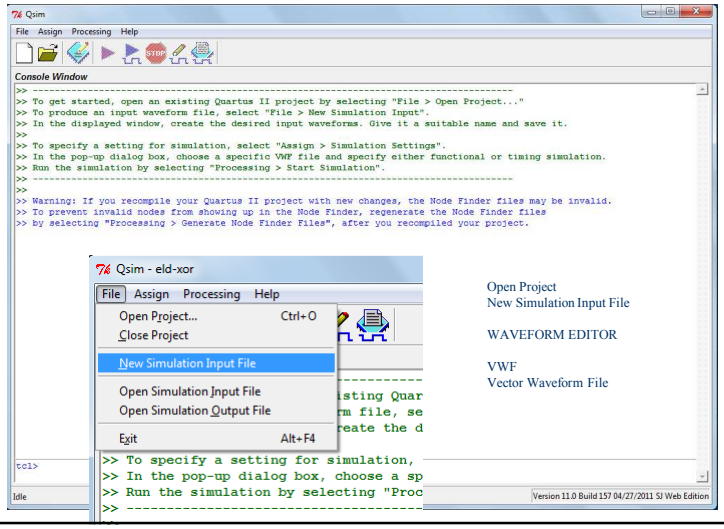


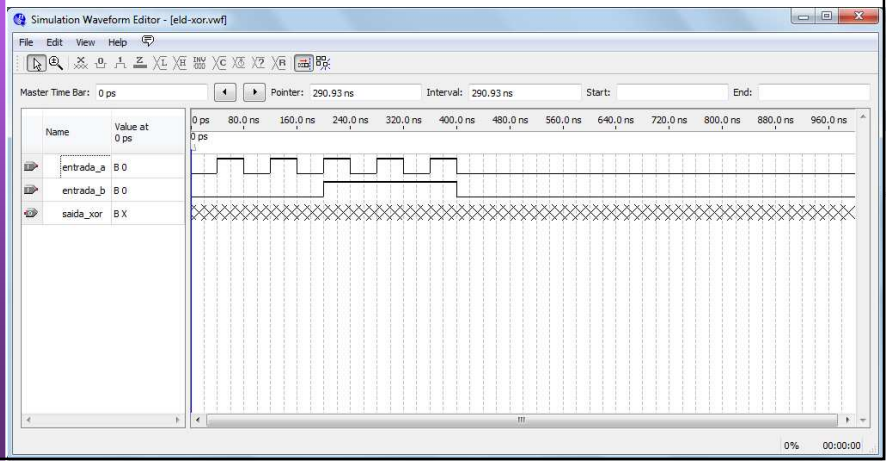
2. Quartus II – Simulação de Circuitos

Simulação de Circuitos: Functional / Timing => Q11 / Q9

Open Project
New Simulation Input File

WAVEFORM EDITOR

VWF
Vector Waveform File



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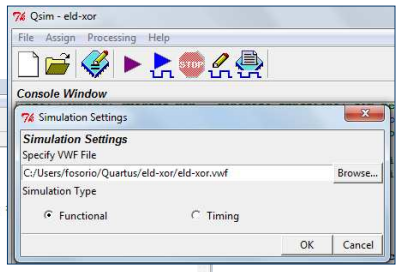
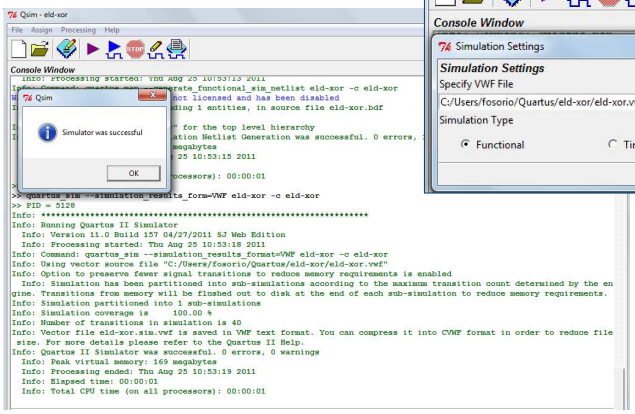
Open Project
New Simulation Input File

WAVEFORM EDITOR

VWF
Vector Waveform File





2. Quartus II – Simulação de Circuitos

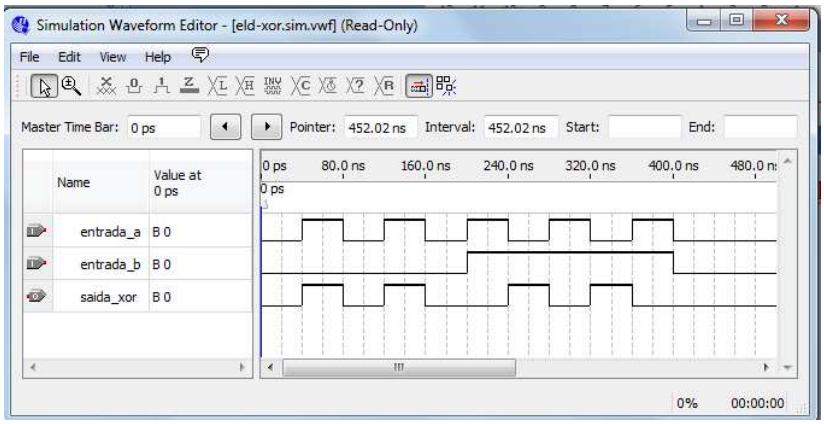
Simulação de Circuitos: Functional / Timing => Q11 / Q9

Open Project
New Simulation Input File

WAVEFORM EDITOR

VWF
Vector Waveform File

RESULTADO DA SIMULAÇÃO



3. Projeto de Circuito em FPGA

Circuitos Lógicos

- XOR
- Half-Adder (meio somador)
- Full-Adder (somador completo)
- Somadores em Cascata

3. Projeto de Circuito em FPGA

Circuitos Lógicos

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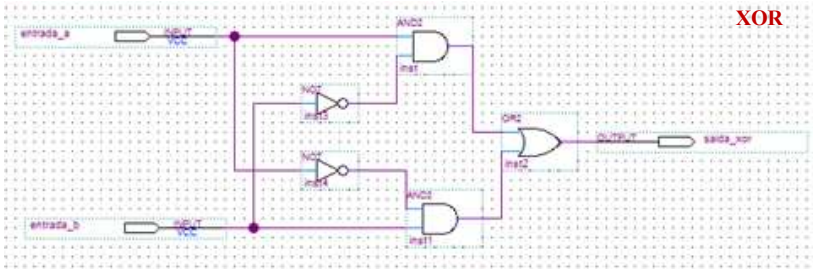
XOR



3. Projeto de Circuito em FPGA

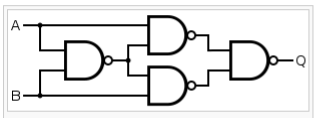
Circuitos Lógicos

- XOR

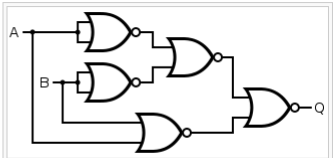
INPUT A	B	OUTPUT A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

SOMA	A + B:
0 + 0 = 0	
0 + 1 = 1	
1 + 0 = 1	
1 + 1 = 0	e vai_um

'ANSI' "Military" XOR Symbol



XOR gate constructed using only NAND gates.

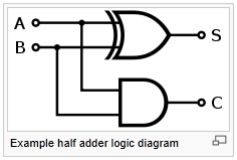


XOR gate constructed using only NOR gates.

3. Projeto de Circuito em FPGA

Circuitos Lógicos

- **Half-Adder**



Example half adder logic diagram

SOMA
A + B = S => XOR

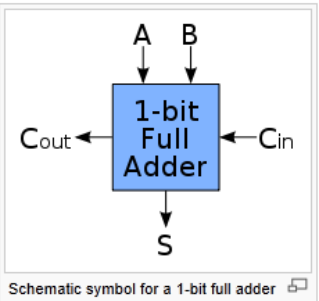
VAI_UM
A + B = C => AND

INPUT A	INPUT B	OUTPUT A XOR B	Vai_Um "Carry"
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3. Projeto de Circuito em FPGA

Circuitos Lógicos

- **Full-Adder**



Schematic symbol for a 1-bit full adder with C_{in} and C_{out} drawn on sides of block to emphasize their use in a multi-bit adder

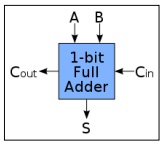
Inputs			Outputs	
A	*B*	C_{in}	C_{out}	*S*
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

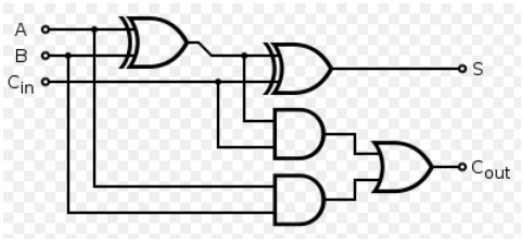
3. Projeto de Circuito em FPGA

Circuitos Lógicos

- **Full-Adder**

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1





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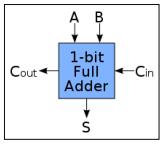
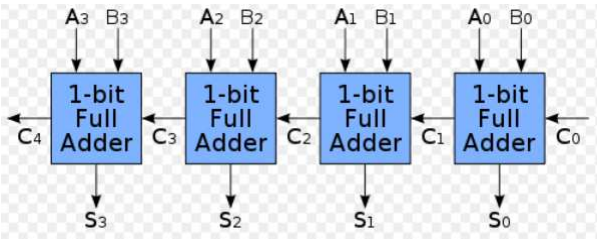
3. Projeto de Circuito em FPGA

Circuitos Lógicos

- **Full-Adder em Cascata: Somador de 4 bits**

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1





Referência – Figuras:
http://en.wikipedia.org/wiki/Adder_(electronics)

INFORMAÇÕES SOBRE A DISCIPLINA

USP - Universidade de São Paulo - São Carlos, SP
ICMC - Instituto de Ciências Matemáticas e de Computação
SSC - Departamento de Sistemas de Computação

LRM – Laboratório de Robótica Móvel
Web LRM: Http://lrm.icmc.usp.br/
Página pessoal: Http://www.icmc.usp.br/ ~fosorio/
E-mail: fosorio [at] { icmc. usp. br , gmail. com } – F.Osório
E-mail: diogosoc [at] { icmc. usp. br } - Diogo Correa (PAE)

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Web Wiki: Http://wiki.icmc.usp.br/index.php/SSC-111
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> Material de Apoio, Trabalhos Práticos