USP - ICMC - SSC
SSC 0111 (Lab ELD I) - 2o. Semestre 2011

Disciplina de Laboratório de Elementos de Lógica Digital I SSC-0111

Prof. Fernando Osório
Email: fosorio [at] { icmc. usp. br , gmail. com }
Estagiário PAE: Diogo Ortiz Correa
Email: diogosoc [at] { icmc. usp. br }
Web: http://www.icmc.usp.br/~fosorio/
Wiki ICMC: http://wiki.icmc.usp.br/index.php/SSC-111(fosorio)

Aula 03

Aula 03 - Introdução

Agenda:

1. Introdução FPGAs
2. Placa DE2-70 – Terasic / Altera
3. Quartus II
4. NIOS II Soft-Processor
5. Projeto de Circuito em FPGA
   Editor de Diagramas Esquemáticos

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices (PLDs / CPLDs)

Tipo de Dispositivos Lógicos Programáveis - [Simple/Complex]PLDs

- **Programmable Logic Array (PLA)**
- **Programmable AND-Array Logic (PAL)**
- **Generic Array Logic (GAL)**
- **PAL, Configurable and Erasable (PALCE)**
- **Field Programmable Gate Array (FPGA)**
- **Programmable Read-Only Memory (PROM)**

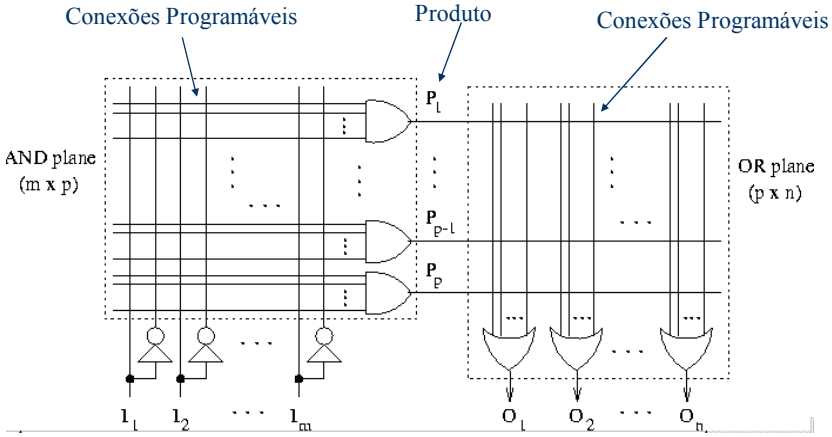
Fonte/Refs.: S. Lee - http://www.postech.ac.kr/class/cs311/ (downloads)
S. Brown and J. Rose - http://www.eecg.toronto.edu/~brown/papers/DandT-FPGA-CPLD.html
http://portal.acm.org/citation.cfm?id=622676

USP – ICMC - SSC0711- Turma 2011/2
Laboratório ELD I BCC-B2 / T04
Prof. Fernando Osório / PAE Diogo Correa

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices (PLDs / CPLDs)

Programmable Logic Array (PLA) - Estrutura Lógica



Fontes.: S. Lee / S.Brown and J. Rose

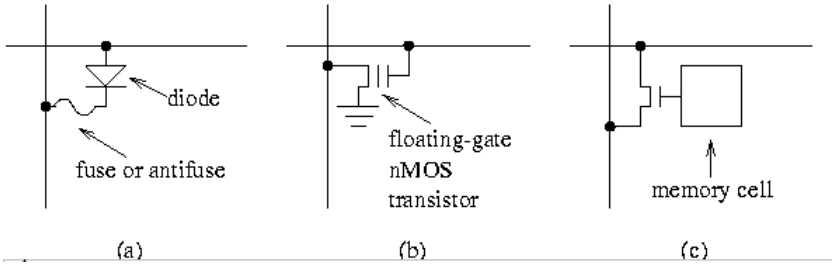
Expressão: Soma dos Produtos

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices (PLDs / CPLDs)

Programmable Logic Array (PLA) - **Métodos de Programação das Conexões**

Usando um programador de PLD (ROM writer)
para programar um PLA: determinar onde as conexões serão feitas.



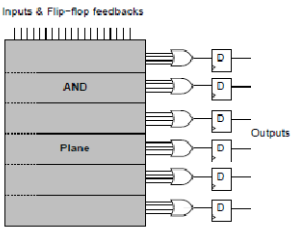
Fontes.: S. Lee / S.Brown and J. Rose

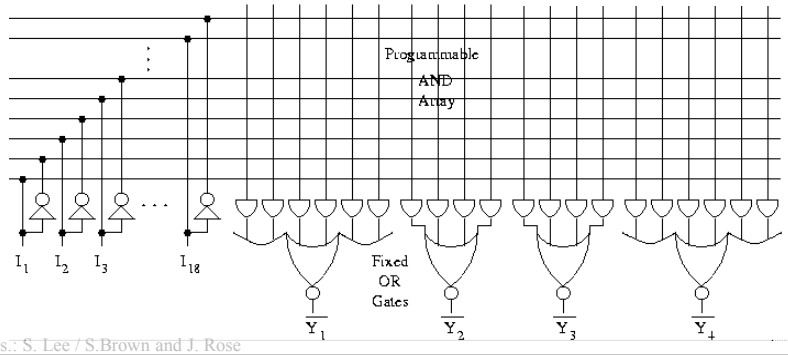
2. Projeto de Hardware Reconfigurável

Programmable Logic Devices

Programmable AND-Array Logic - **PAL**

PAL- Programmable Array Logic (PAL) is a relatively small FPD that has a programmable AND-plane followed by a fixed OR-plane [PAL is a trademark of Advanced Micro Devices]





Fontes.: S. Lee / S.Brown and J. Rose

2. Projeto de Hardware Reconfigurável

Programmable Logic Devices

Field Programmable Gate Arrays - FPGA

- A maioria dos tipos de chips complexos pode ser "programado" para implementar circuitos arbitrários;
- Diferentes fabricantes competindo entre si: Actel, Altera, Cypress, Lattice, Xilinx, etc.
- Fatores competitivos:
  - Grande nro. de portas lógicas;
  - Velocidade dos dispositivos;
  - Flexibilidade e Custo;
  - Reprogramabilidade;

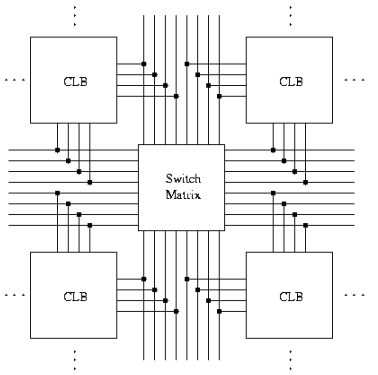
> FPGA: um array programável de PLDs simples
> FPGA: field programmable version of "gate array"

Fontes.: S. Lee / S.Brown and J. Rose

3. FPGA - Field Programmable Gate Array

FPGA - XC4010XL Xilinx FPGA Block Diagram

FPGA: CLB + Interconnection Logic
CLB = Combinatorial/Configurable Logic Block (Elemento básico)



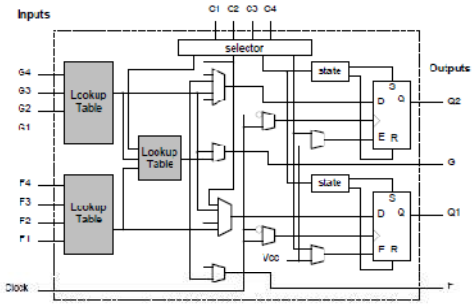
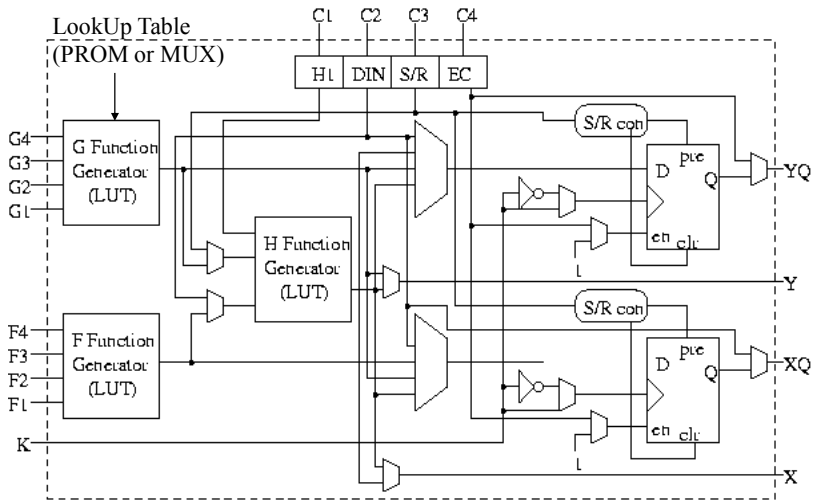


Figure 18 - *Xilinx XC4000 Configurable Logic Block (CLB).*

3. FPGA - Field Programmable Gate Array

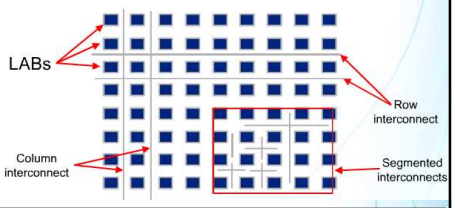
FPGA - XC4010XL Xilinx FPGA - CLB Block Diagram

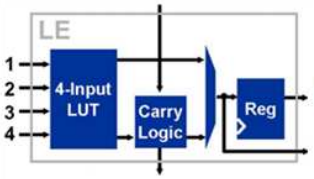


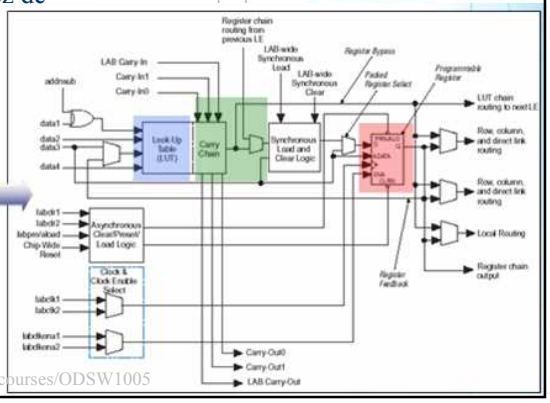
3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA

Altera CLPDs => FPGA
LAB - Logic Array Blocks
FPGA LAB composto de
Logic Elements (LE), em vez de
Produto de Termos
e MacroCélulas







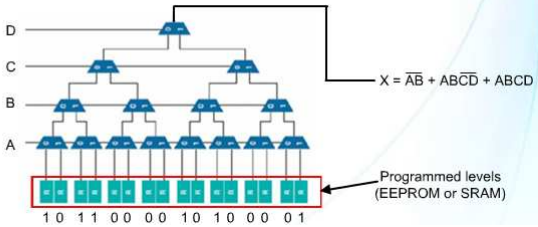
Material Complementar:
Altera FPGA Curso On-Line
http://www.altera.com/education/training/courses/ODSW1005

3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA

Altera CLPDs => FPGA
LAB - Logic Array Blocks
FPGA LAB composto de Logic Elements (LE)
Logic Element LUTs,

LUT inputs are mux select lines



3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA - Cyclone EP1C**

Table 1. Cyclone Device Overview

Feature	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Logic Elements (LEs)	2,910	4,000	5,980	12,060	20,060
M4K RAM Blocks (4 Kbits + parity)	13	17	20	52	64
Total RAM Bits	59,904	78,336	92,160	239,616	294,912
Phase-Locked Loops (PLLs)	1	2	2	2	2
Maximum User I/O Pins	104	301	185	249	301
Production Device Availability	April 2003	September 2003	Now	Now	Now

Cyclone™ microtronix ALTERA firefly Configurable Processor Module

Hardware - SCE 703:
Cyclone I - EP1C12F324C8
Firefly Board
NIOS II

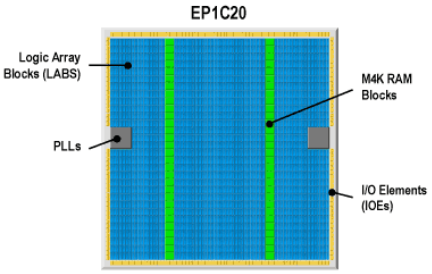
Site Altera Cyclone: http://www.altera.com/products/devices/cyclone/cyc-index.jsp

FPGA - Altera FPGA - Cyclone EP1C20

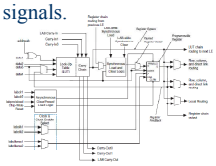
Cyclone Architecture

Abundant logic and memory resources, clock management circuitry, and advanced I/O capabilities are all available in Cyclone devices. The Cyclone architecture consists of vertically arranged Logic Elements (LEs), embedded memory blocks, and phase-locked loops (PLLs) that are surrounded by I/O elements (IOEs). A highly efficient interconnect and low-skew clock network provide connectivity between each of these structures for clock and data signals.

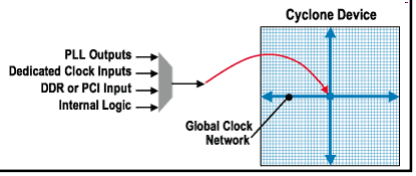
EP1C20 Device Floorplan



Cyclone LE Logic Element



Cyclone Device Clock Network

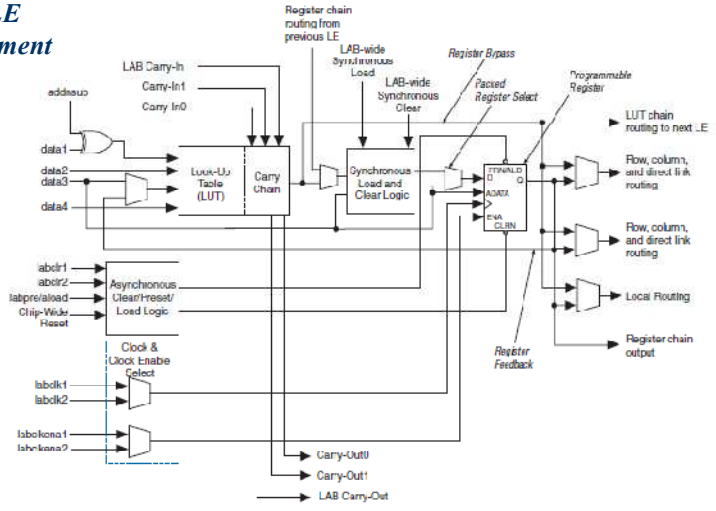


USP – ICMC - SSC0711- Turma 2011/2
Laboratório ELD I BCC-B2 / T04
Prof. Fernando Osório / PAE Diogo Correa

3. FPGA - Field Programmable Gate Array

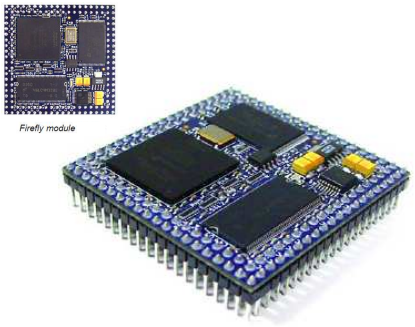
FPGA - Altera FPGA - Cyclone EP1C20

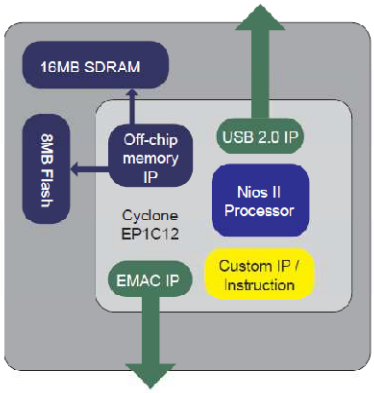
Cyclone LE Logic Element



3. FPGA - Field Programmable Gate Array

FPGA - Altera FPGA - Cyclone EP1C12 Kit - Firefly





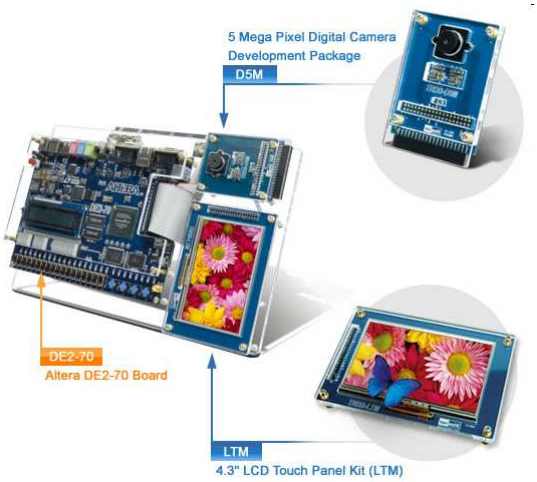
Firefly Configurable Processing Modules add FPGA flexibility and 32-bit RISC processing power to your next embedded product.

Firefly modules can be designed to fit any number of embedded device requirements

Site Microtronix Firefly: http://www.microtronix.com/downloads/?product_id=88

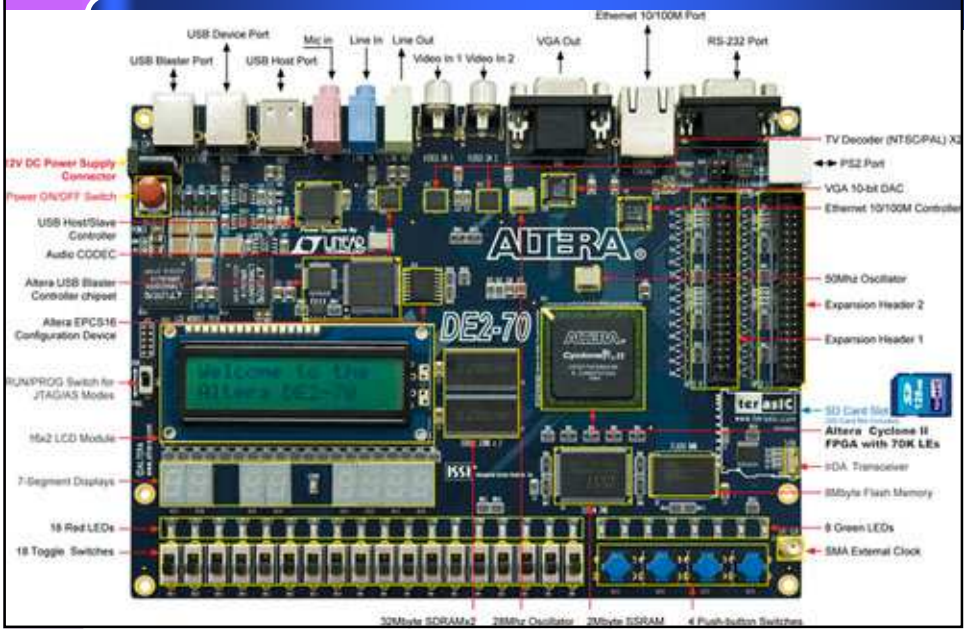
4. DE2-70

Sistemas Embarcados - Exemplo do DE2-70 / DM5 / LTM



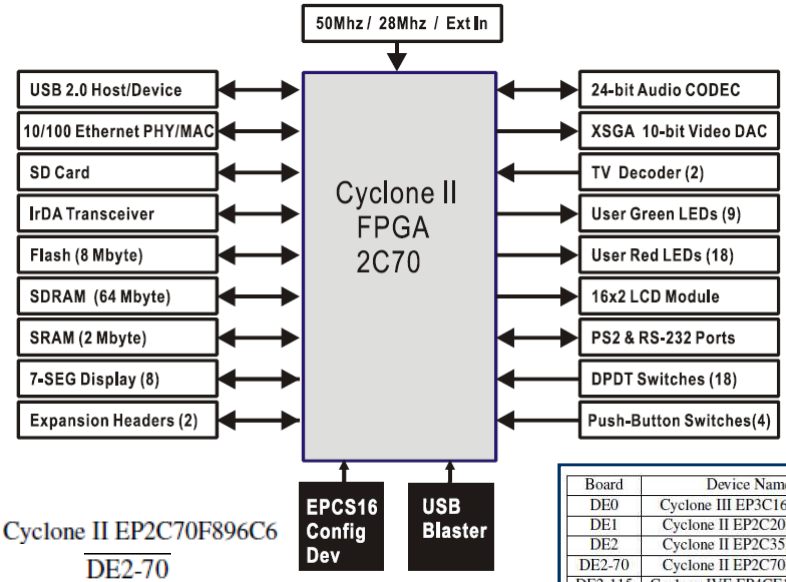
Site: http://www.terasic.com.tw/cgi-bin/page/archive.pl?CategoryNo=39

Placa DE2-70 – Terasic / Altera



USP – ICMC - SSC0711- Turma 2011/2
Laboratório ELD I BCC-B2 / T04
Prof. Fernando Osório / PAE Diogo Correa

Placa DE2-70 – Terasic / Altera



Cyclone II EP2C70F896C6

DE2-70

Block diagram of the DE2-70

Board	Device Name
DE0	Cyclone III EP3C16F484C6
DE1	Cyclone II EP2C20F484C7
DE2	Cyclone II EP2C35F672C6
DE2-70	Cyclone II EP2C70F896C6
DE2-115	Cyclone IVE EP4CE115F29C7

Table 1. DE-series FPGA device names

4. Altera FPGA

Ferramentas de Desenvolvimento

Ferramentas de Software

Quartus II 9.0 – 11.0 Altera (Web Edition)
SOPC Builder and IP Solutions
Nios II Integrated Development Environment (IDE) - Cyclone Edition

Simulator

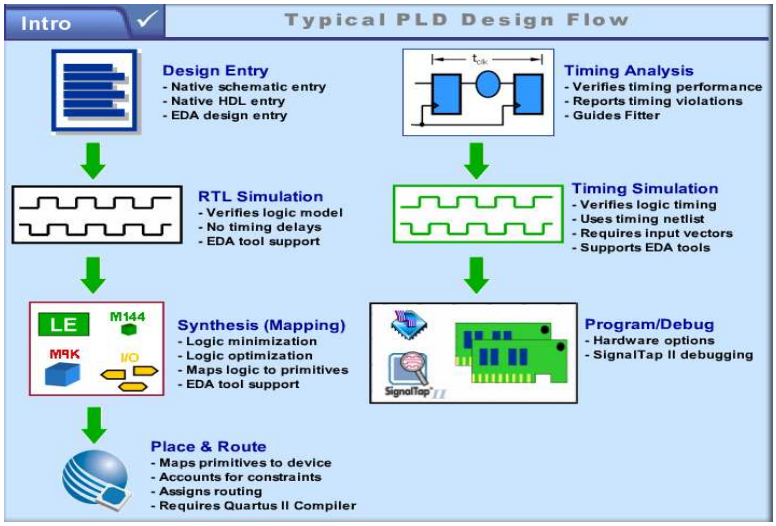
Ferramentas de Hardware

Altera FPGA EP2C70F896C6
Cyclone II – Terasic DE2-70 Board
NIOS II Kit (Soft-Processor)

USP – ICMC - SSC0711- Turma 2011/2
Laboratório ELD I BCC-B2 / T04
Prof. Fernando Osório / PAE Diogo Correa

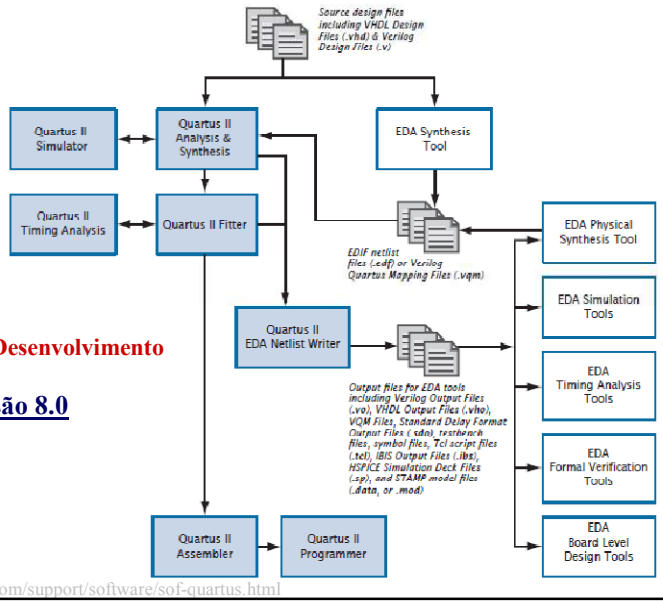
4. Altera FPGA

Ferramentas de Desenvolvimento



4. Altera FPGA

EDA Tool Design Flow



Ferramentas de Desenvolvimento

Quartus II Versão 8.0

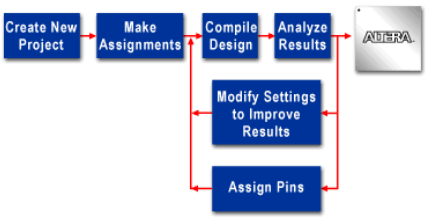
Site http://www.altera.com/support/software/sof-quartus.html

4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0

Quartus II Software Basic Design Flow



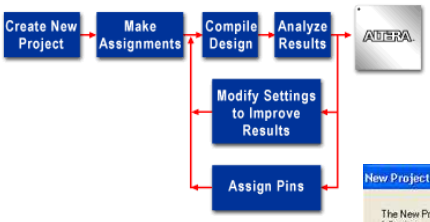
Site http://www.altera.com/support/software/sof-quartus.html

4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0

Quartus II Software Basic Design Flow



>> New Project Wizard

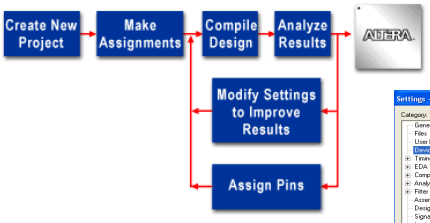
USP – ICMC - SSC0711- Turma 2011/2
Laboratório ELD I BCC-B2 / T04
Prof. Fernando Osório / PAE Diogo Correa

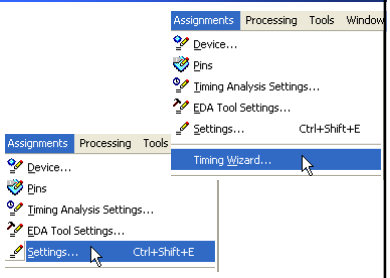
4. Altera FPGA

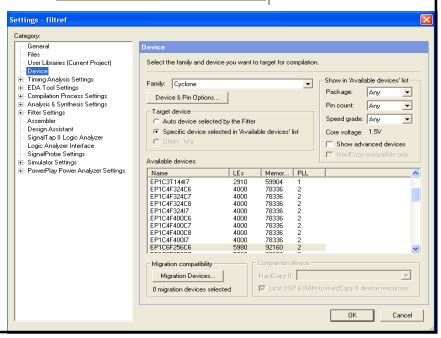
Ferramentas de Desenvolvimento

Quartus II Versão 8.0

Quartus II Software Basic Design Flow







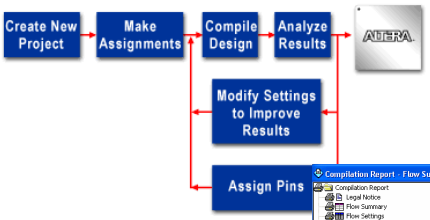
>> Assignments Menu:
Settings, Timing

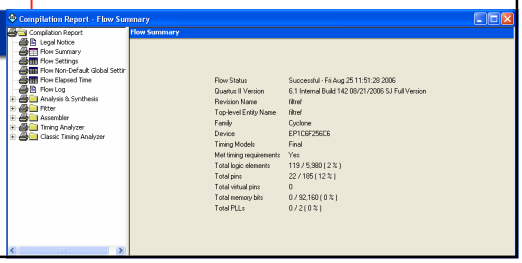
4. Altera FPGA

Ferramentas de Desenvolvimento

Quartus II Versão 8.0

Quartus II Software Basic Design Flow



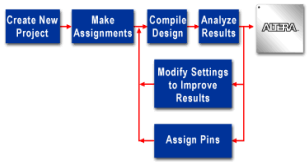


>> Compile Design and Analyze Results

4. Altera FPGA

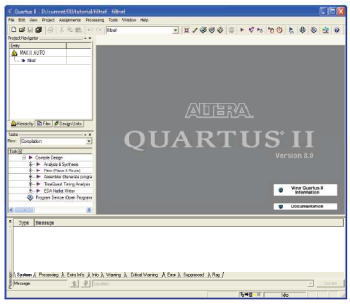
Quartus II Versão 8.0

Quartus II Software Basic Design Flow



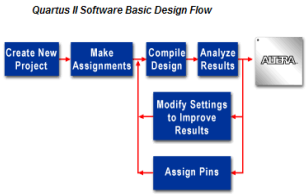
Steps:

1. Create New Project
   New Project Wizard
   > Add Files (vhd, v)
   > Create Block Diagram Schematic File
   Block Editor (bdf)
   MegaFunctions (MegaWizard)
   > Add Pins
2. Make Assignments
   Settings (clock speed)
   Timing Wizard
   > Assignment Editor
   > Timing Analysis
3. Compile Design
4. Analyze Results
5. Modify Settings to Improve Results (Timing Analysis)
6. Assign Pins (Assignment Editor)



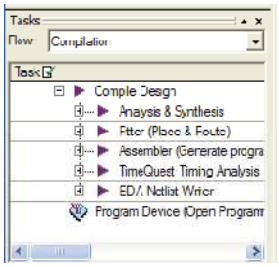
4. Altera FPGA

Quartus II Versão 8.0



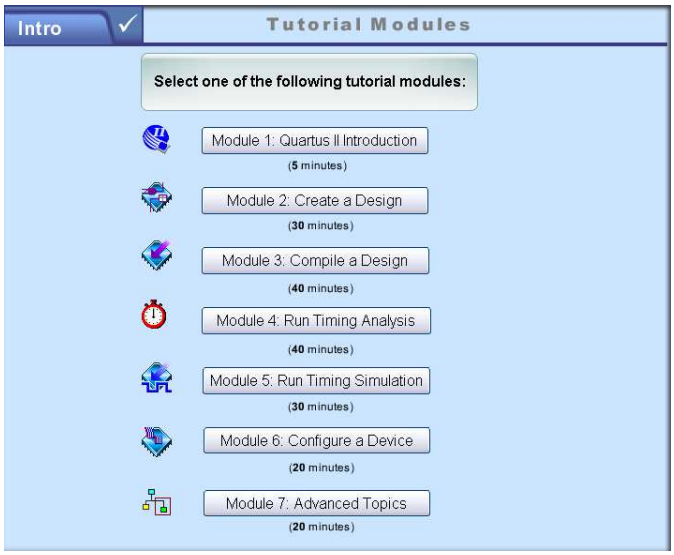
Steps:

1. Create New Project
   New Project Wizard
   > Add Files (vhd, v)
   > Create Block Diagram Schematic File
   Block Editor (bdf)
   MegaFunctions (MegaWizard)
   > Add Pins
2. Make Assignments
   Settings (clock speed)
   Timing Wizard
   > Assignment Editor
   > Timing Analysis
3. **Compile Design**
4. Analyze Results
5. Modify Settings to Improve Results (Timing Analysis)
6. Assign Pins (Assignment Editor)



4. Altera FPGA

Quartus II Versão 8.0 - TUTORIAL



4. Bibliografia

Laboratório de ELD I

- Bibliografia

Bibliografia Básica:

- BROWN, S. ; VRANESIC, Z. Fundamentals of Digital Logic with VHDL Design, McGraw Hill, 2000.

- IDOETA,I.V.; CAPUANO, F.G. Elementos de Eletrônica Digital, 12 ed., São Paulo, Livros Érica, Livros, 1987

- TAUB, H.; SCHILLING, D. Eletrônica Digital, McGraw-Hill do Brasil, 1982.

* Ver Site da Altera:
http://www.altera.com/education/univ/materials/boards/de2-70/unv-de2-70-board.html

http://www.altera.com/education/univ/materials/digital_logic/tutorials/unv-tutorials.html
Quartus II Introduction Using Schematic Designs

Universidade de São Paulo - São Carlos,SP
Instituto de Ciências Matemáticas e de Computação

INFORMAÇÕES SOBRE A DISCIPLINA

USP - Universidade de São Paulo - São Carlos, SP
ICMC - Instituto de Ciências Matemáticas e de Computação
SSC - Departamento de Sistemas de Computação

LRM – Laboratório de Robótica Móvel
Web LRM: Http://lrm.icmc.usp.br/
Página pessoal: Http://www.icmc.usp.br/ ~fosorio/
E-mail: fosorio [at] { icmc. usp. br , gmail. com } – F.Osório
E-mail: diogosoc [at] { icmc. usp. br } - Diogo Correa (PAE)

Disciplina de Laboratório de Elementos de Lógica Digital I [LELD1]
Web Disciplinas: Http://www.icmc.usp.br/~fosorio/
Web Wiki: Http://wiki.icmc.usp.br/index.php/SSC-111
> Programa, Material de Aulas, Critérios de Avaliação,
> Material de Apoio, Trabalhos Práticos