Elementos de Lógica Digital II

Aula 4 – Introduction to Moore FSM

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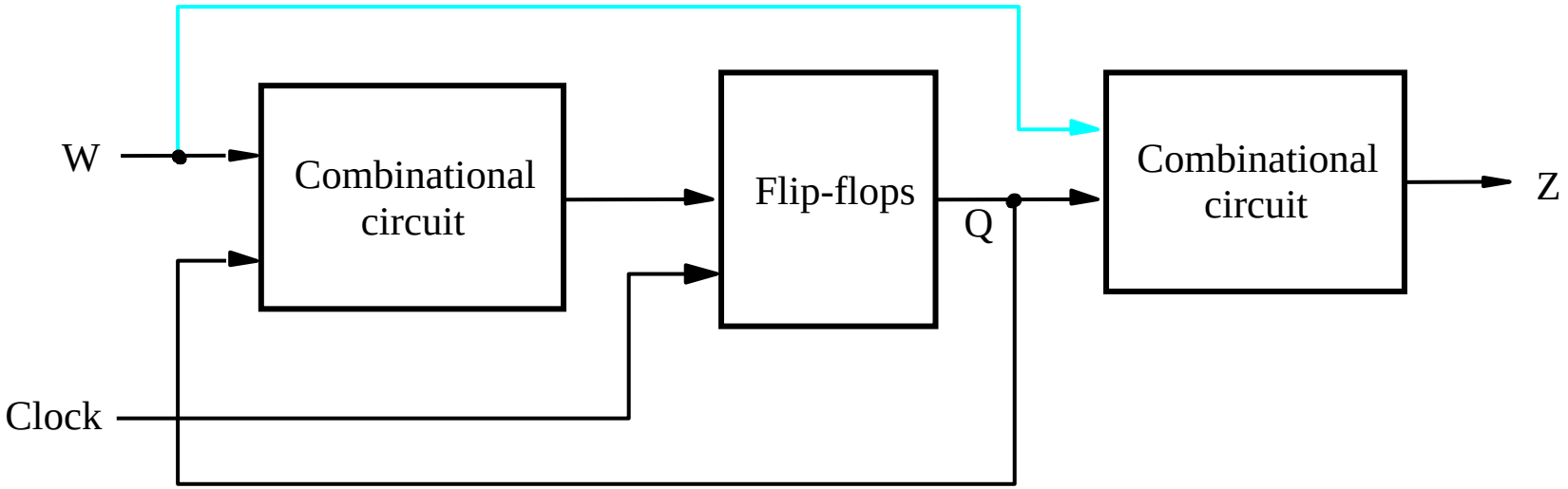

Figure 8.1. The general form of a sequential circuit.

Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0

Figure 8.2. Sequences of input and output signals.

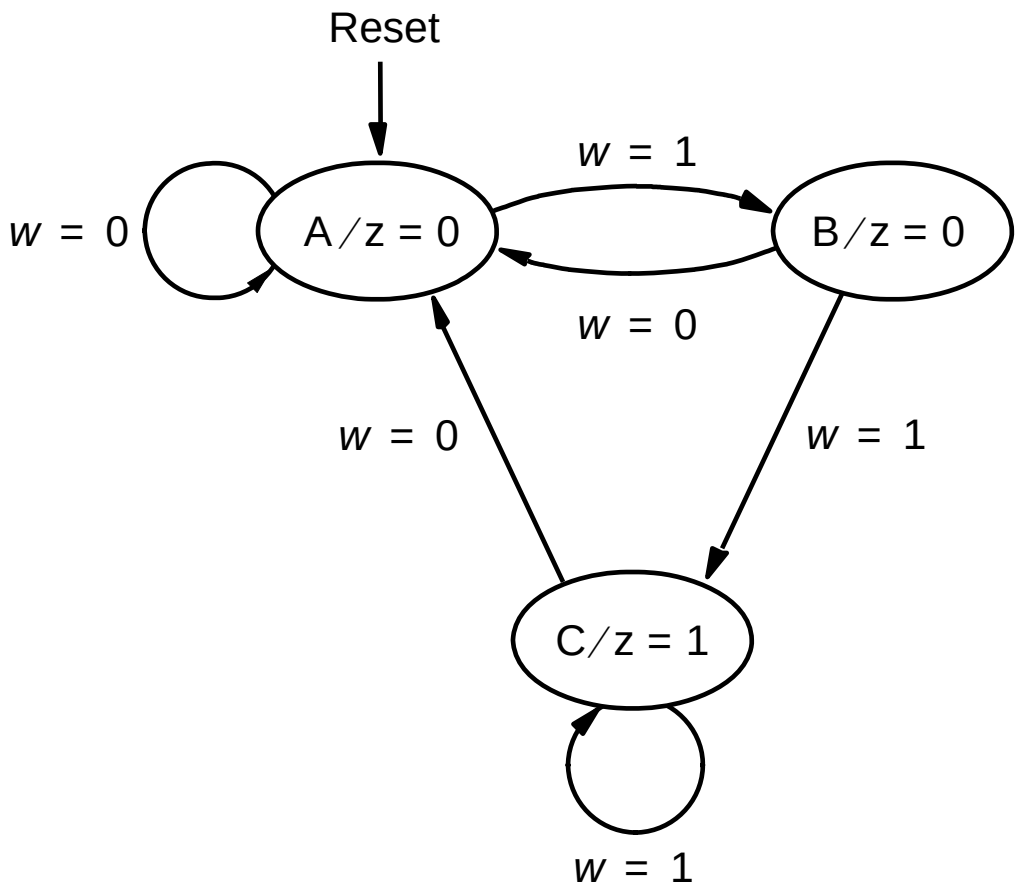

Figure 8.3. State diagram of a simple sequential circuit.

Present state	Next state		Output
	$w = 0$	$w = 1$	z
A	A	B	0
B	A	C	0
C	A	C	1

Figure 8.4. State table for the sequential circuit in Figure 8.3.

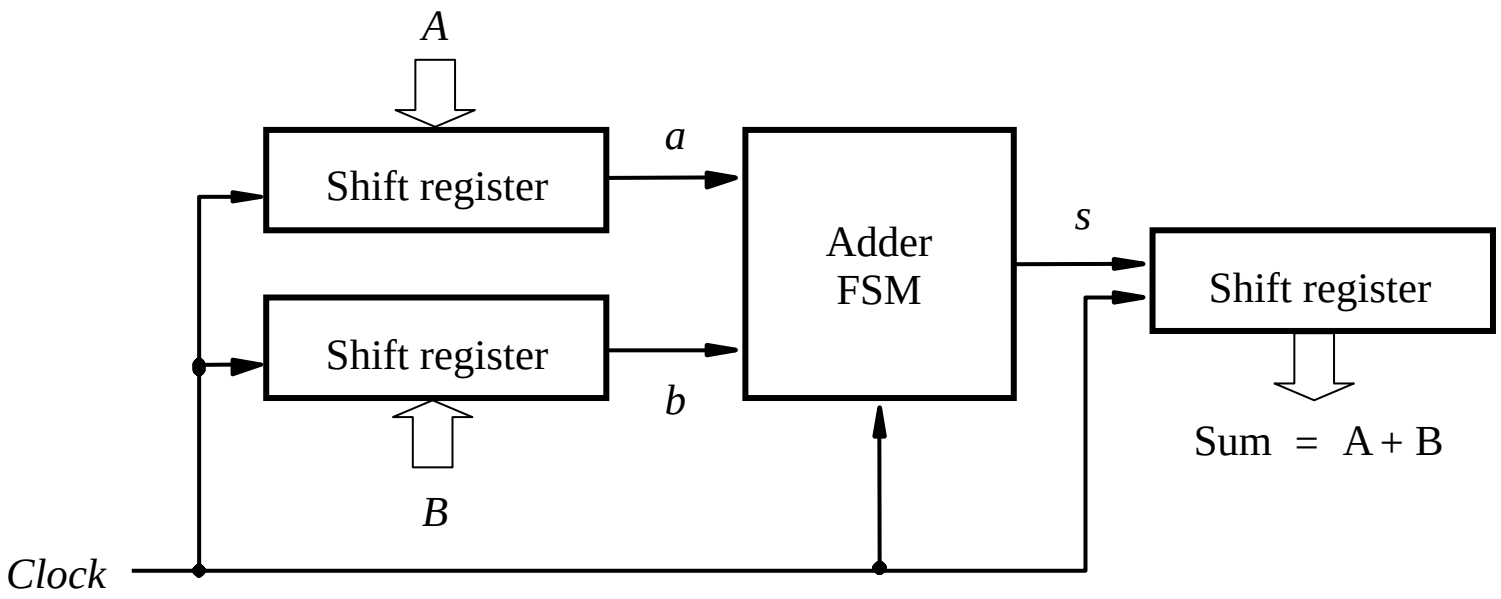

Figure 8.39. Block diagram for the serial adder.

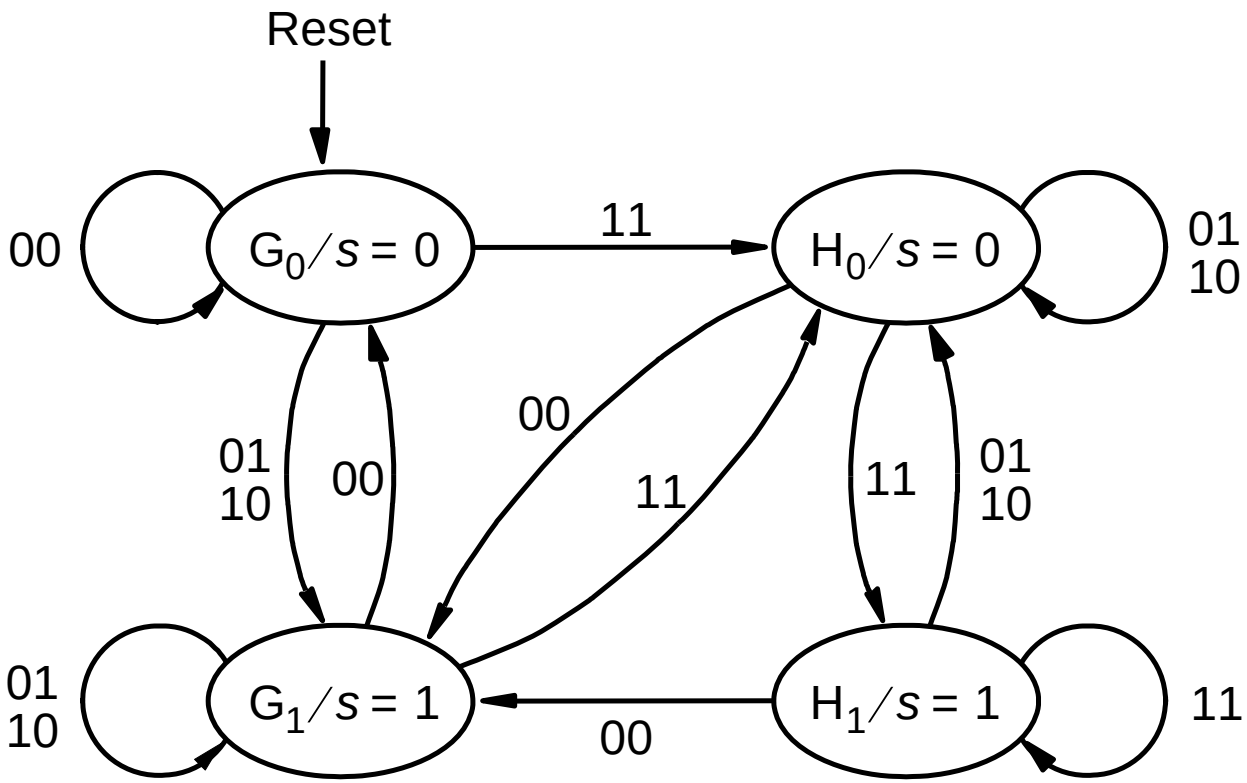

Figure 8.44. State diagram for the Moore-type serial adder FSM.