SCE 0110 -
Elementos de Lógica Digital I

Flip-Flops, Registradores e Contadores (continuacao)

Prof. Dr. Vanderlei Bonato

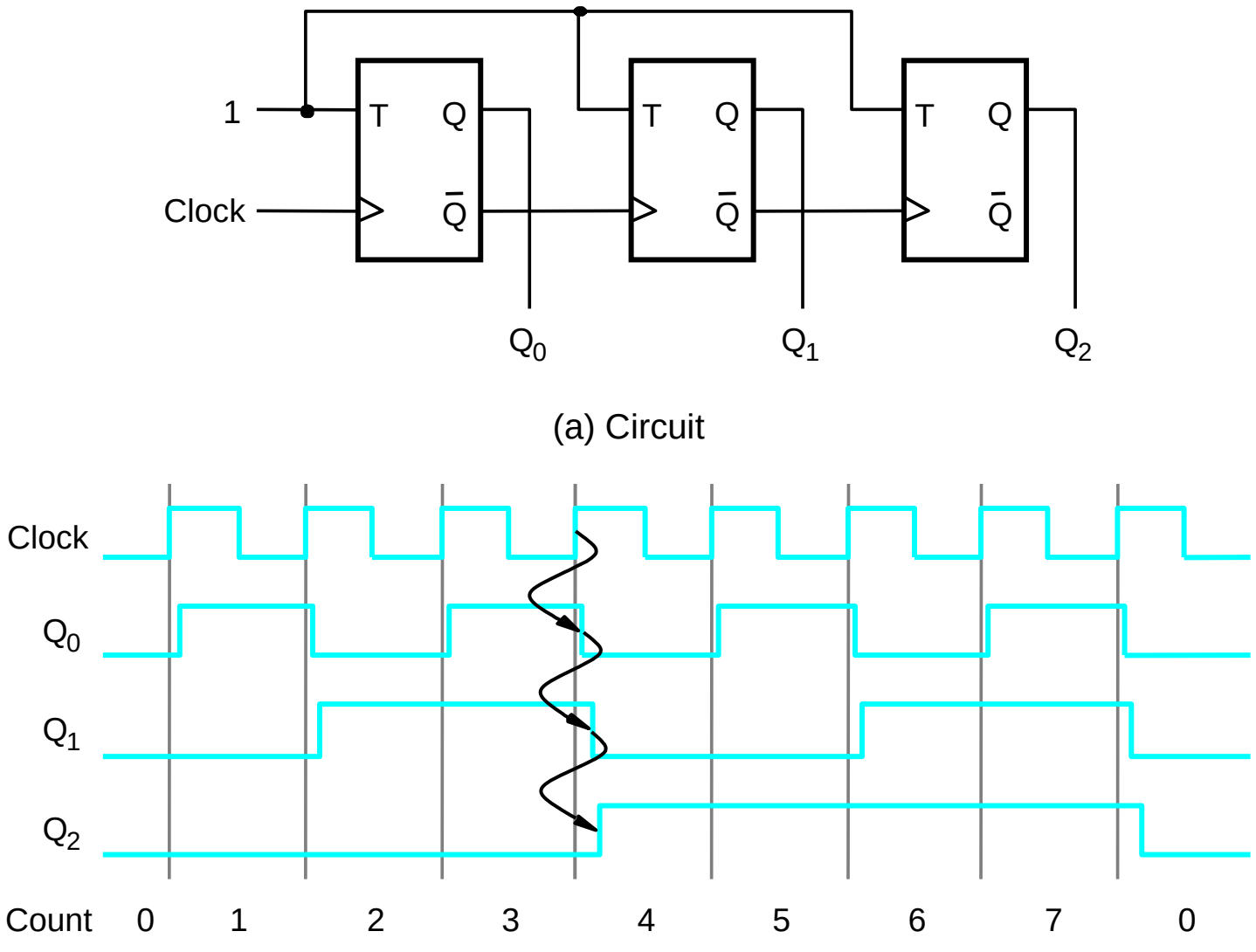

Figure 7.20. A three-bit up-counter.

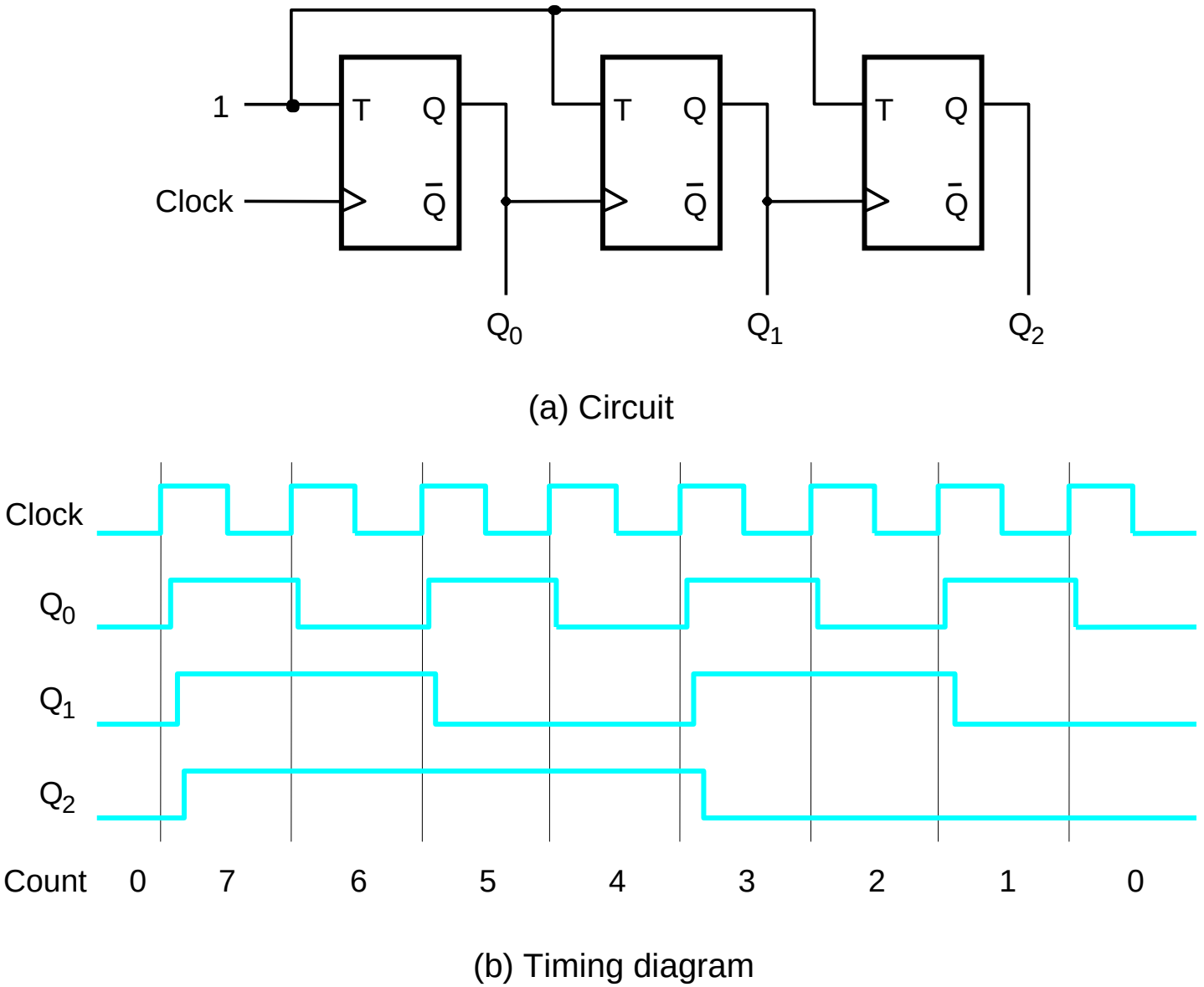

Figure 7.21. A three-bit down-counter.

Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

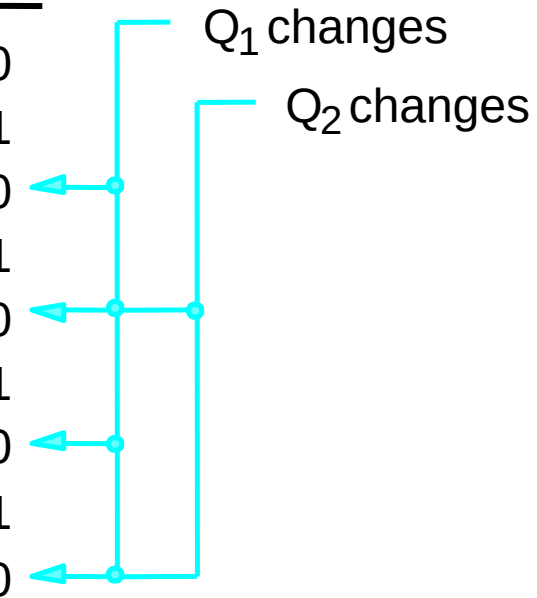

Table 7.1. Derivation of the synchronous up-counter.

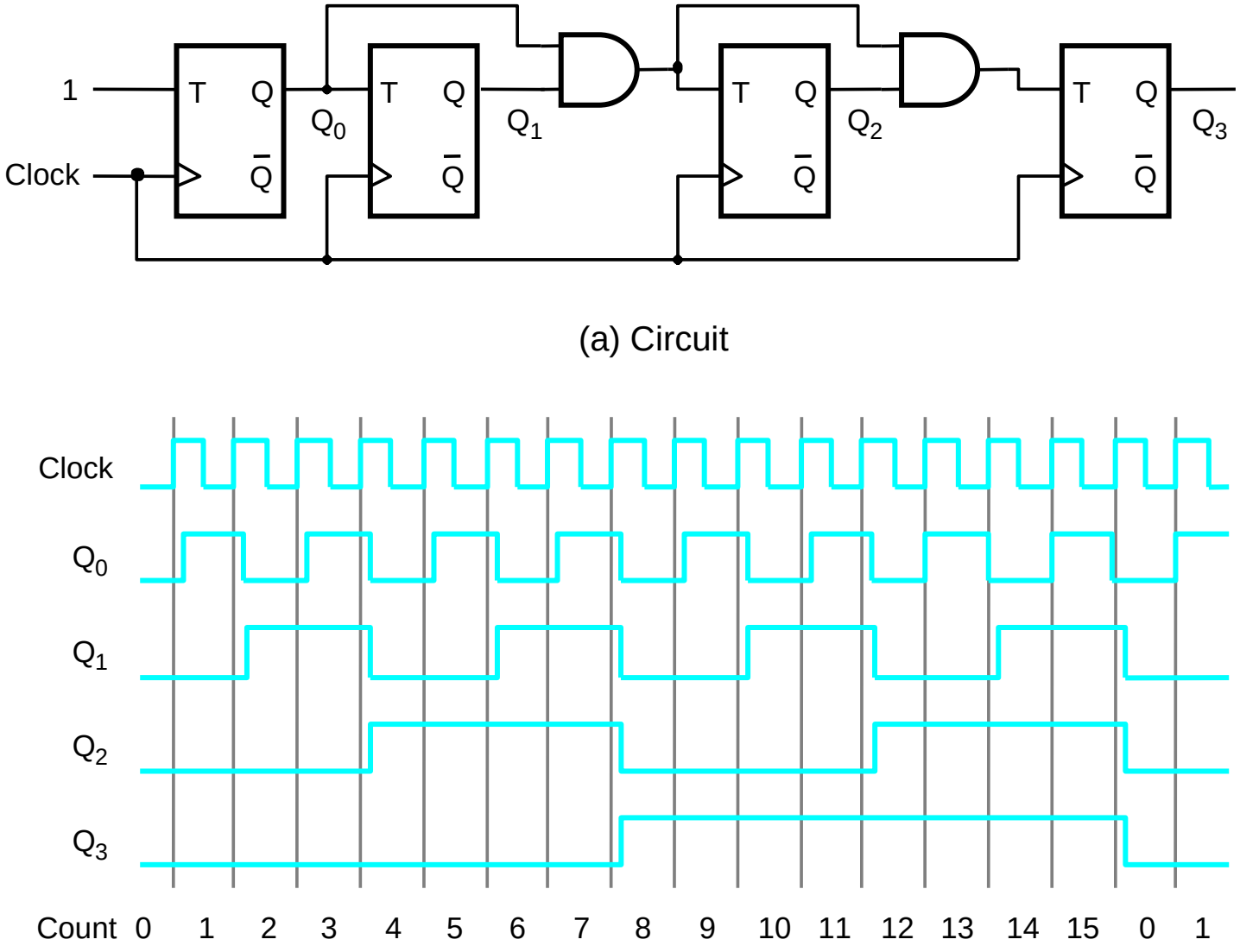

Figure 7.22. A four-bit synchronous up-counter.

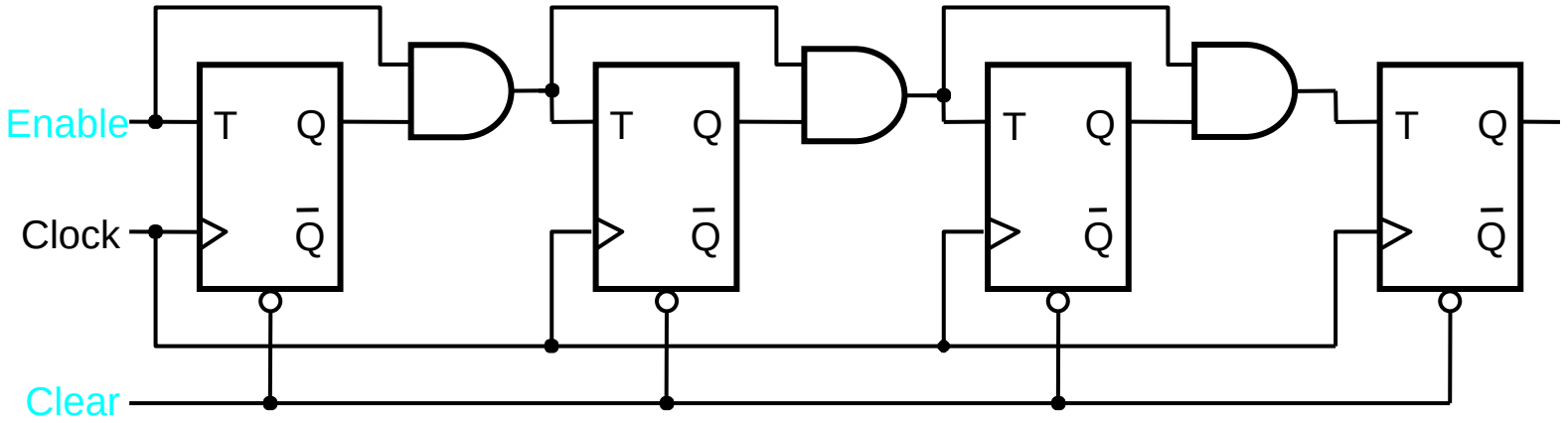

Figure 7.23. Inclusion of Enable and Clear capability.