SCE 0110 -
Elementos de Lógica Digital I

Tecnologia de Implementação (continuação)

Prof. Vanderlei Bonato

Sumário

- FPGAs e outros dispositivos lógicos programáveis
- Estrutura física de um transistor do tipo MMOS
- Vídeo de uma fábrica virtual de CIs

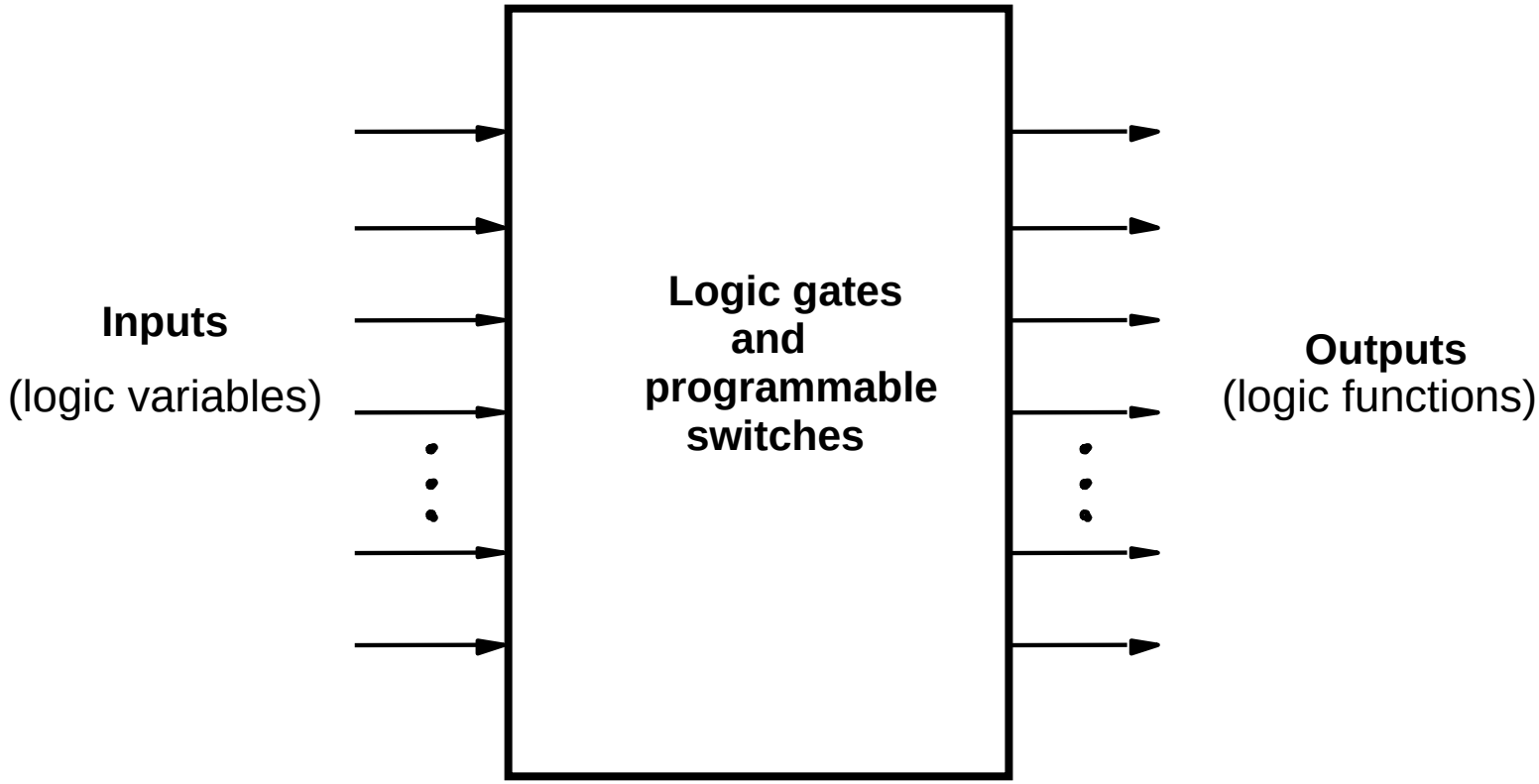


Figure 3.24. Programmable logic device as a black box.

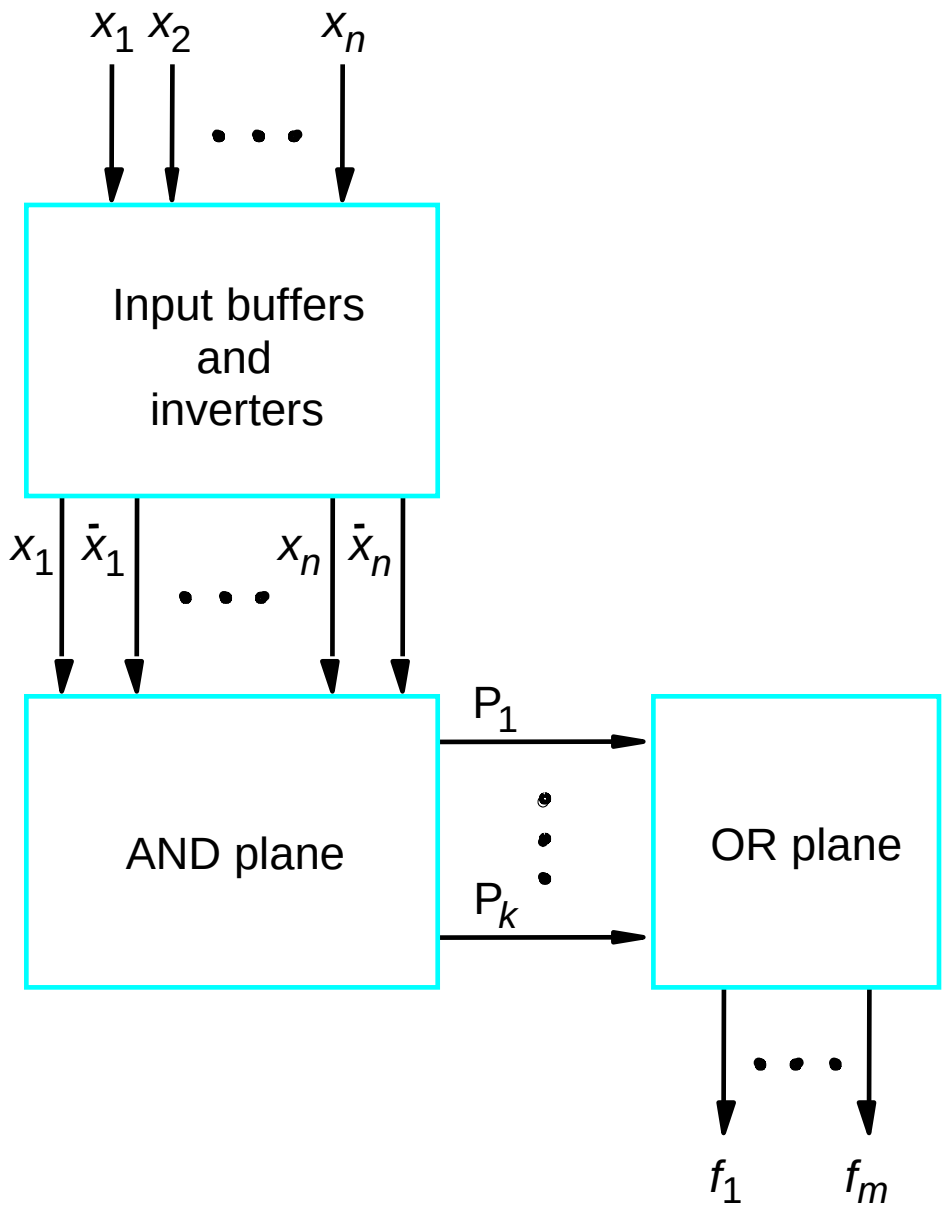


Figure 3.25. General structure of a PLA.

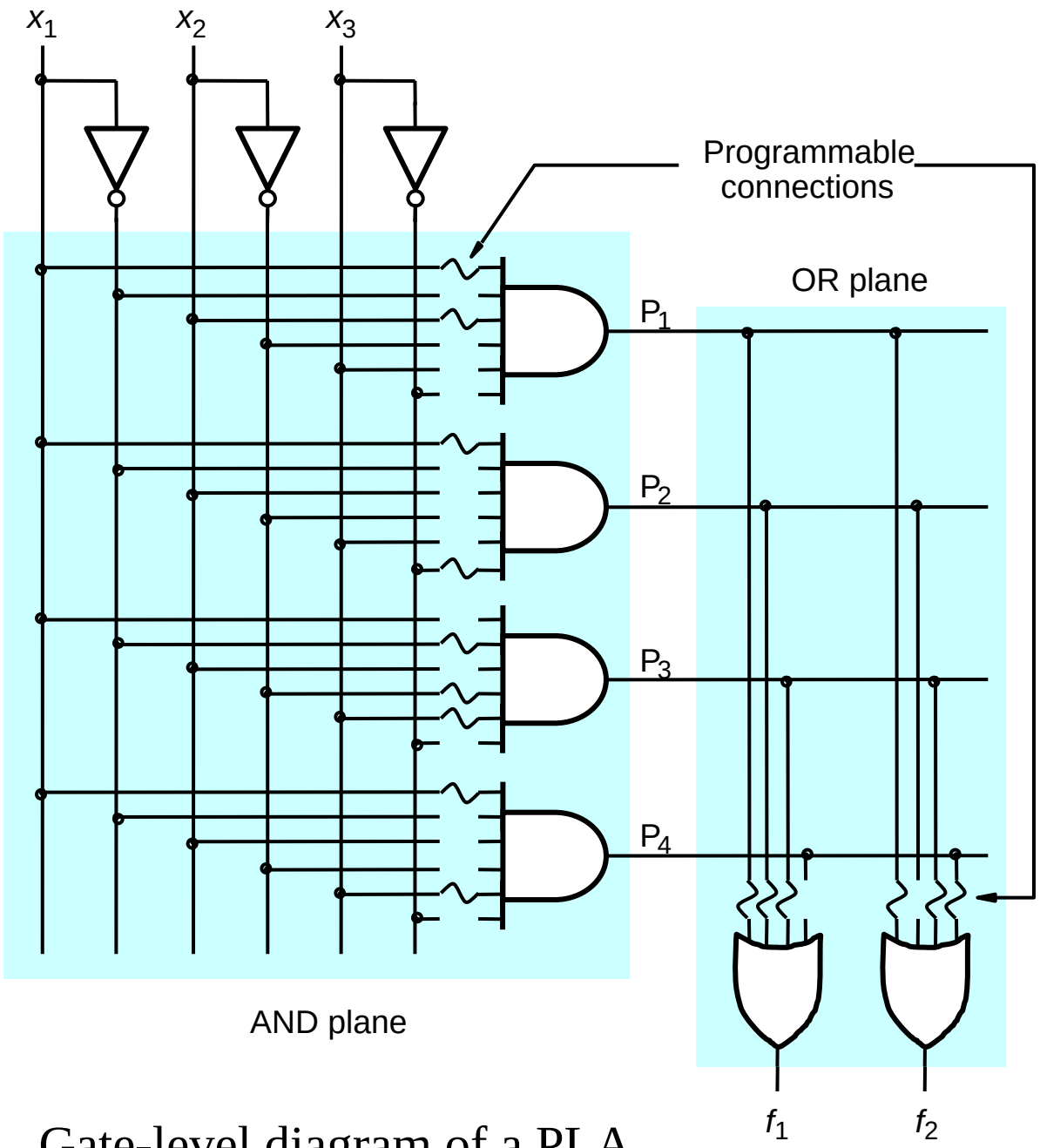


Figure 3.26. Gate-level diagram of a PLA.

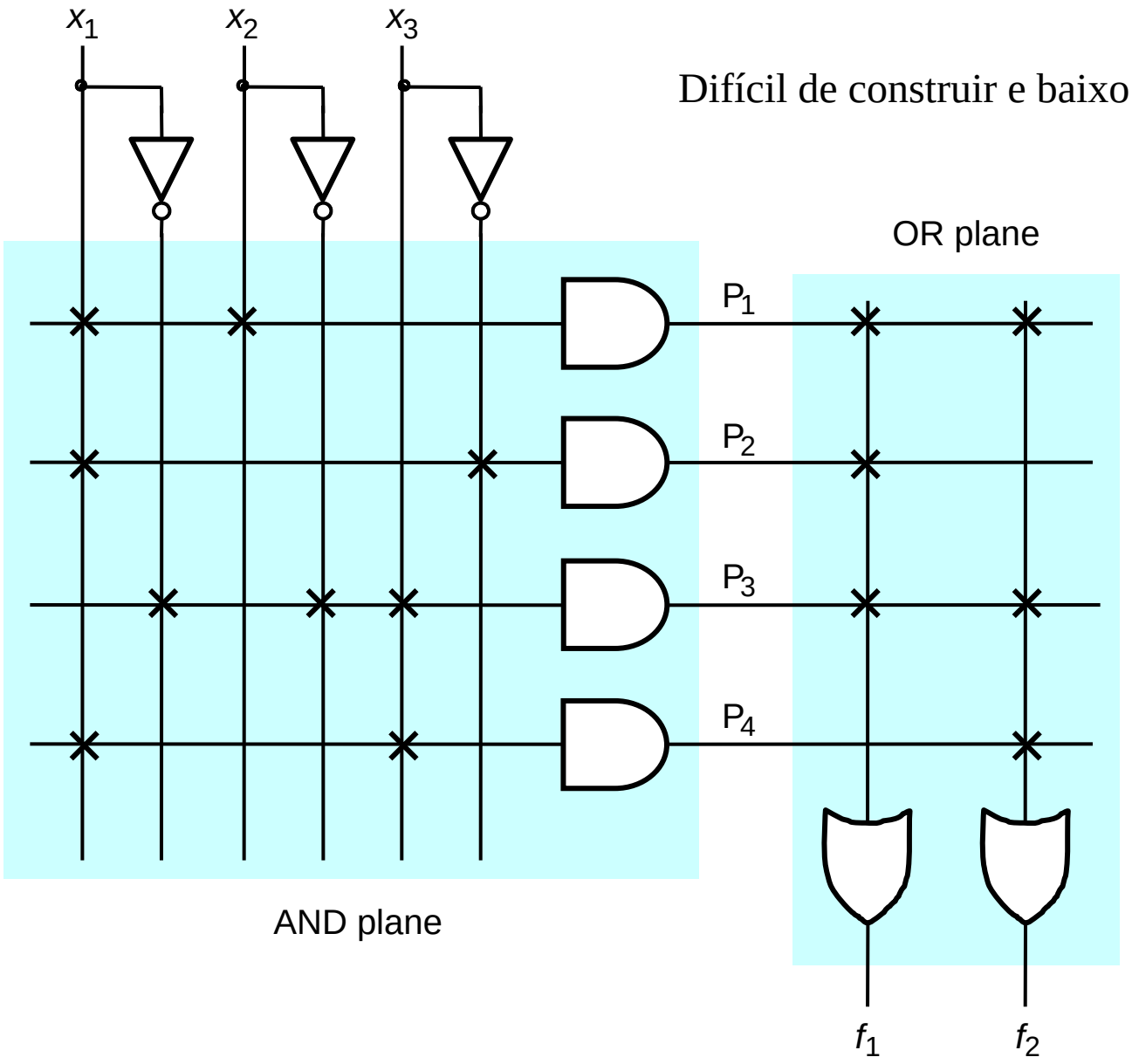


Figure 3.27. Customary schematic for the PLA in Figure 3.26.

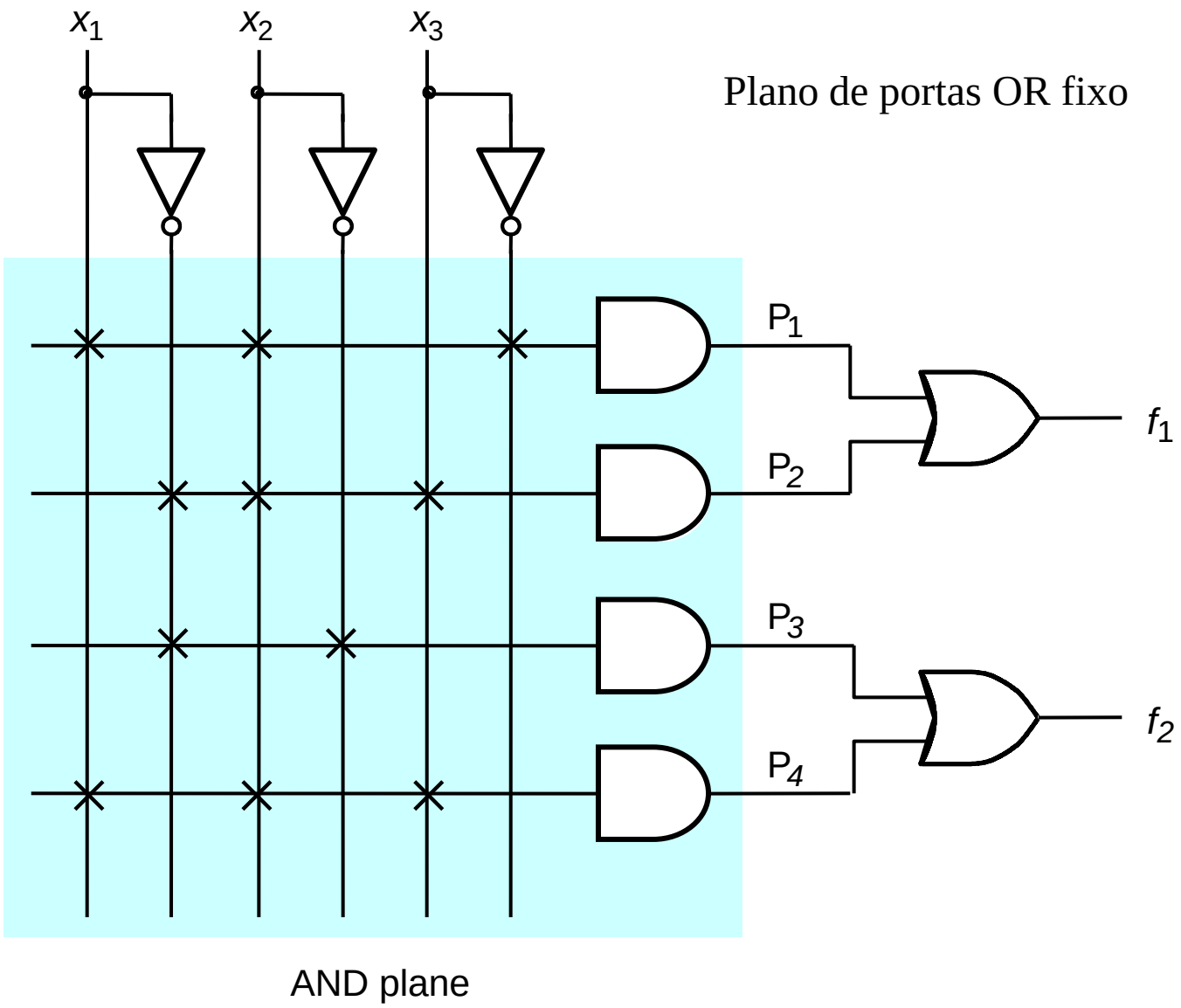


Figure 3.28. An example of a PAL

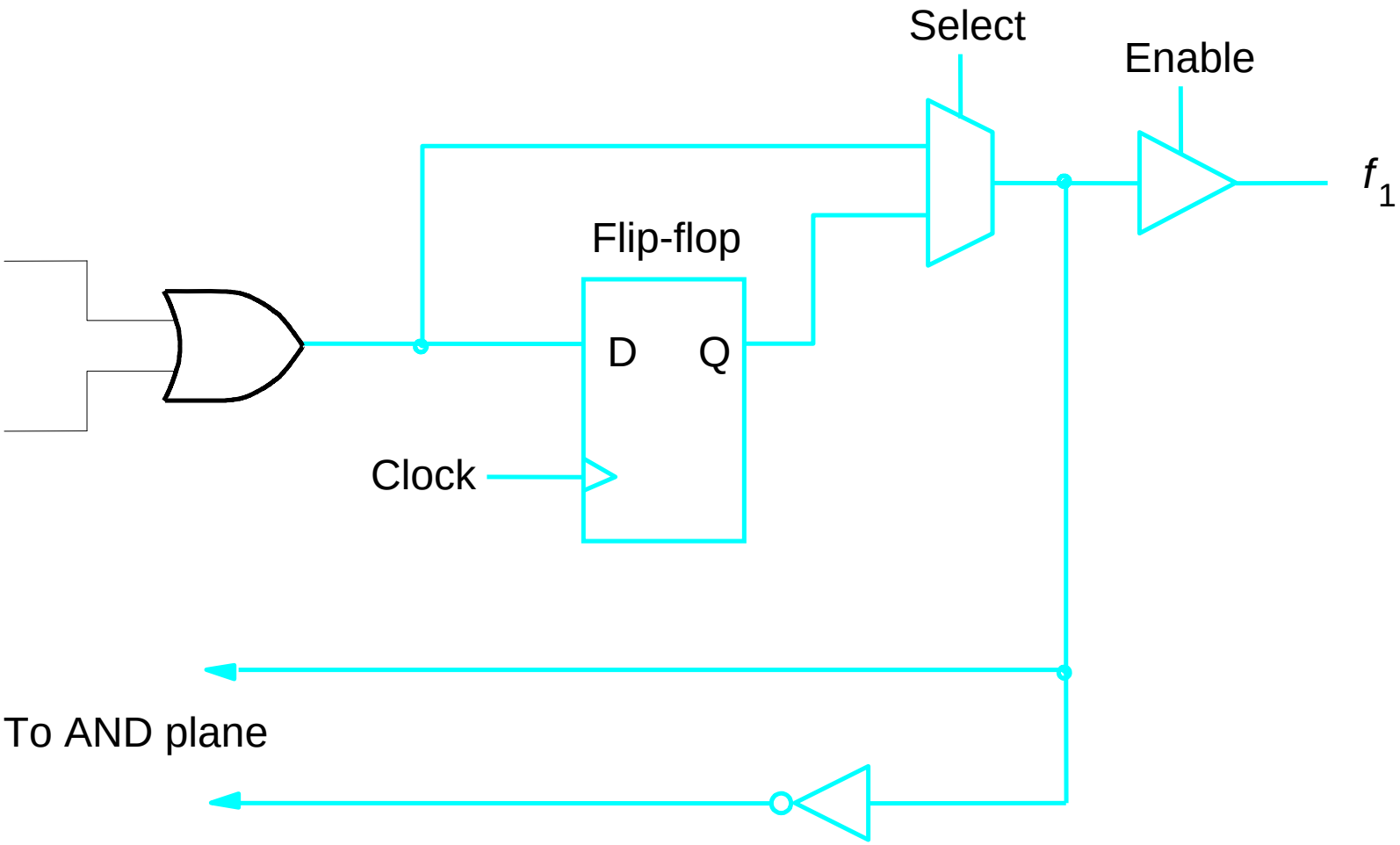


Figure 3.29. Extra circuitry added to OR-gate from Figure 3.28.

Figure 3.30. A PLD programming unit (courtesy of Data IO Corp).

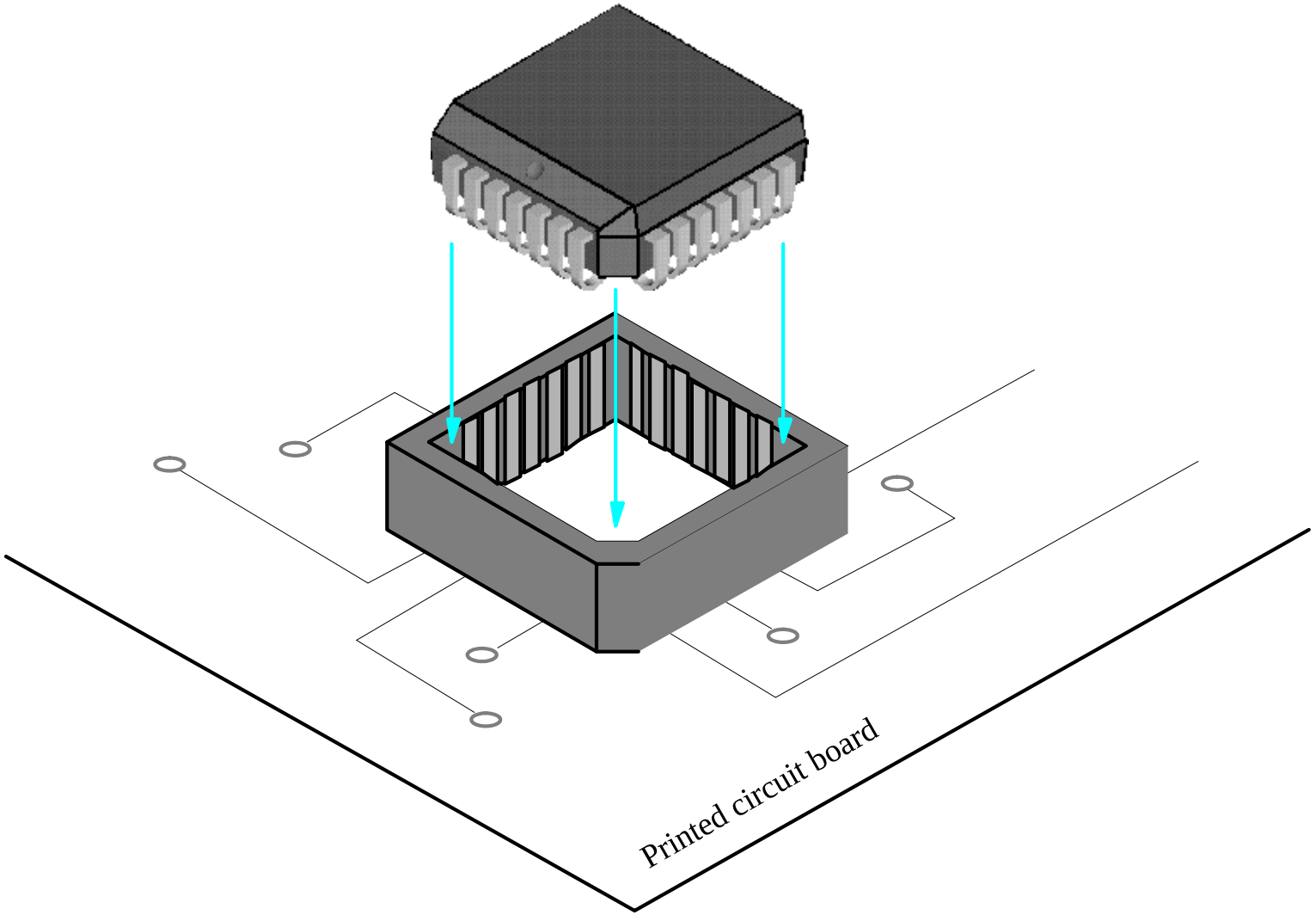


Figure 3.31. A PLCC package with socket.

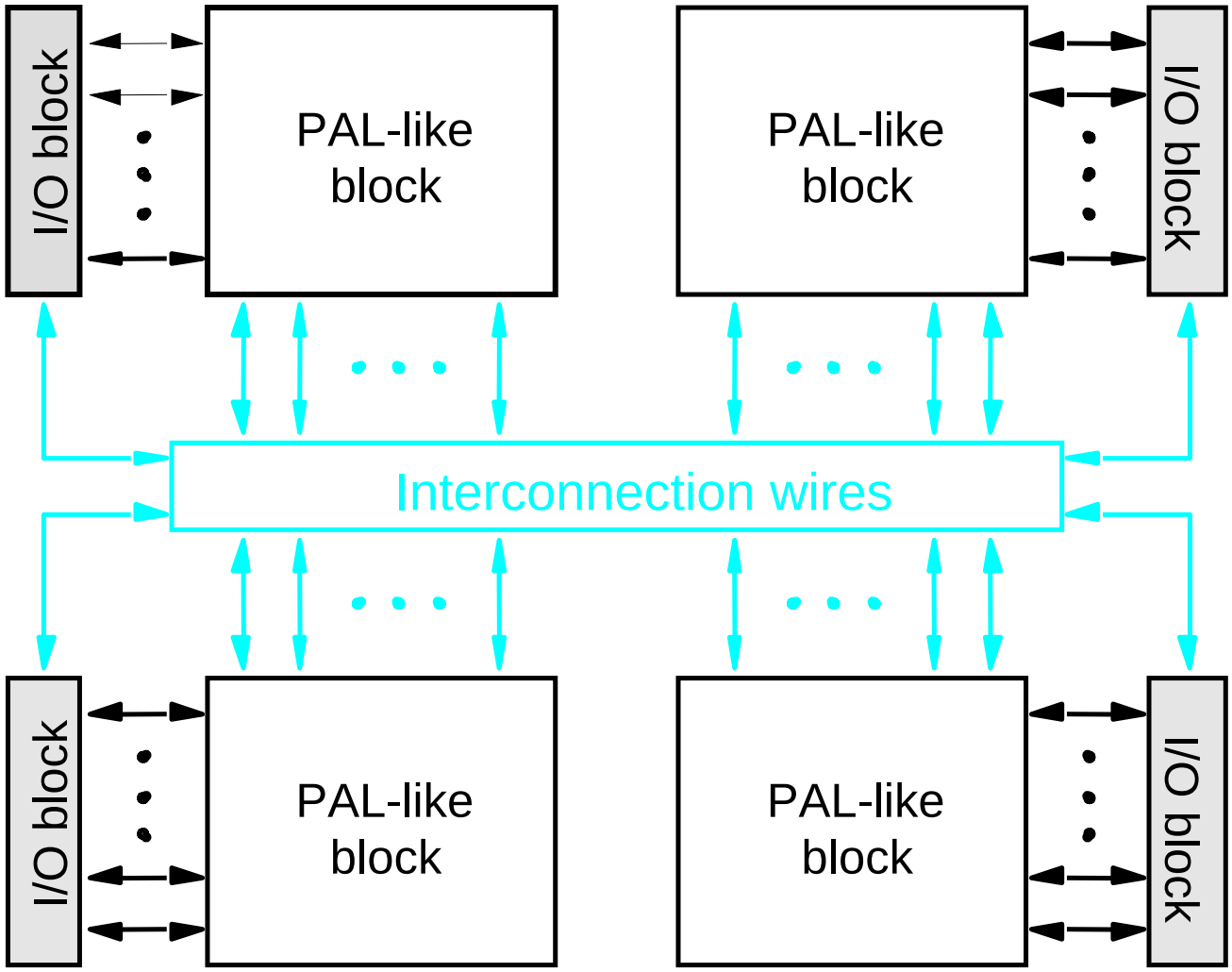


Figure 3.32. Structure of a complex programmable logic device (CPLD).

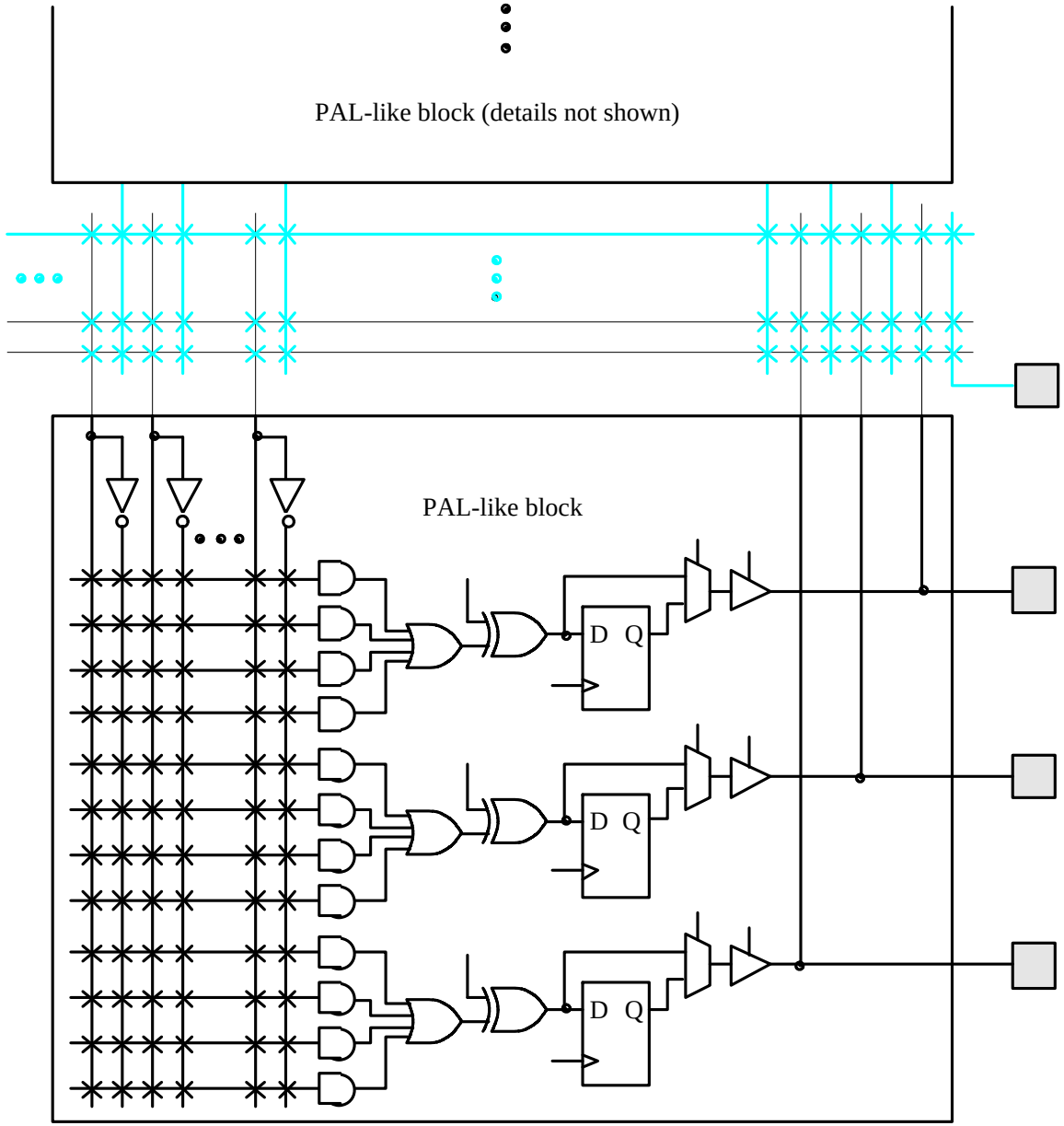
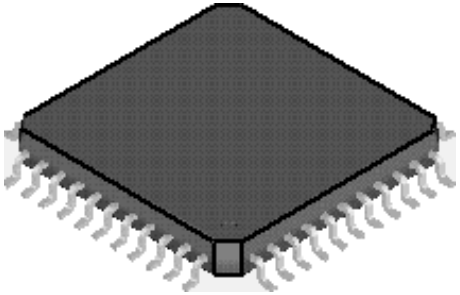
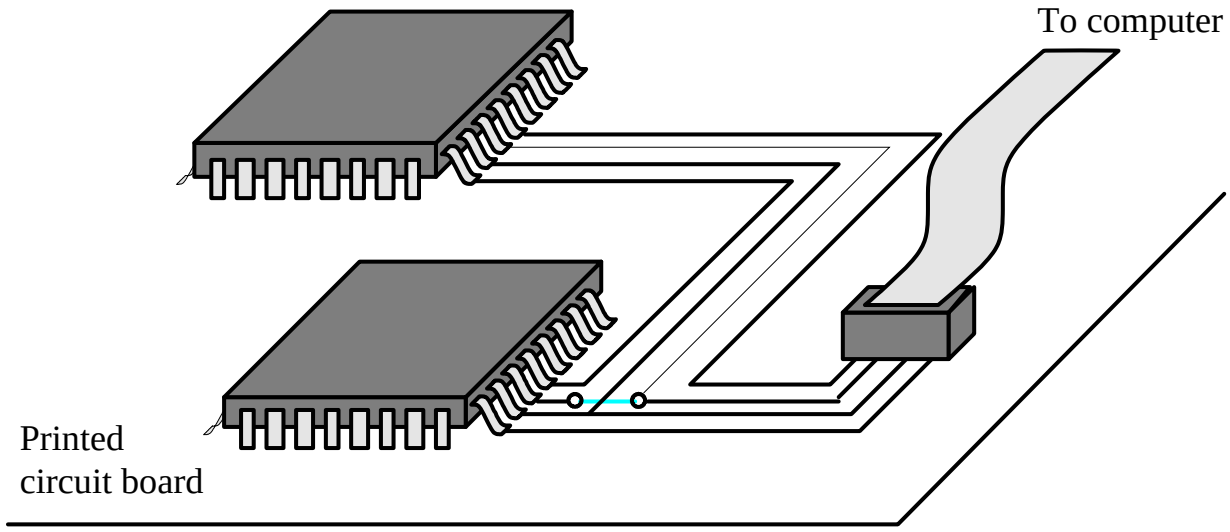


Figure 3.33. A section of the CPLD in Figure 3.32.

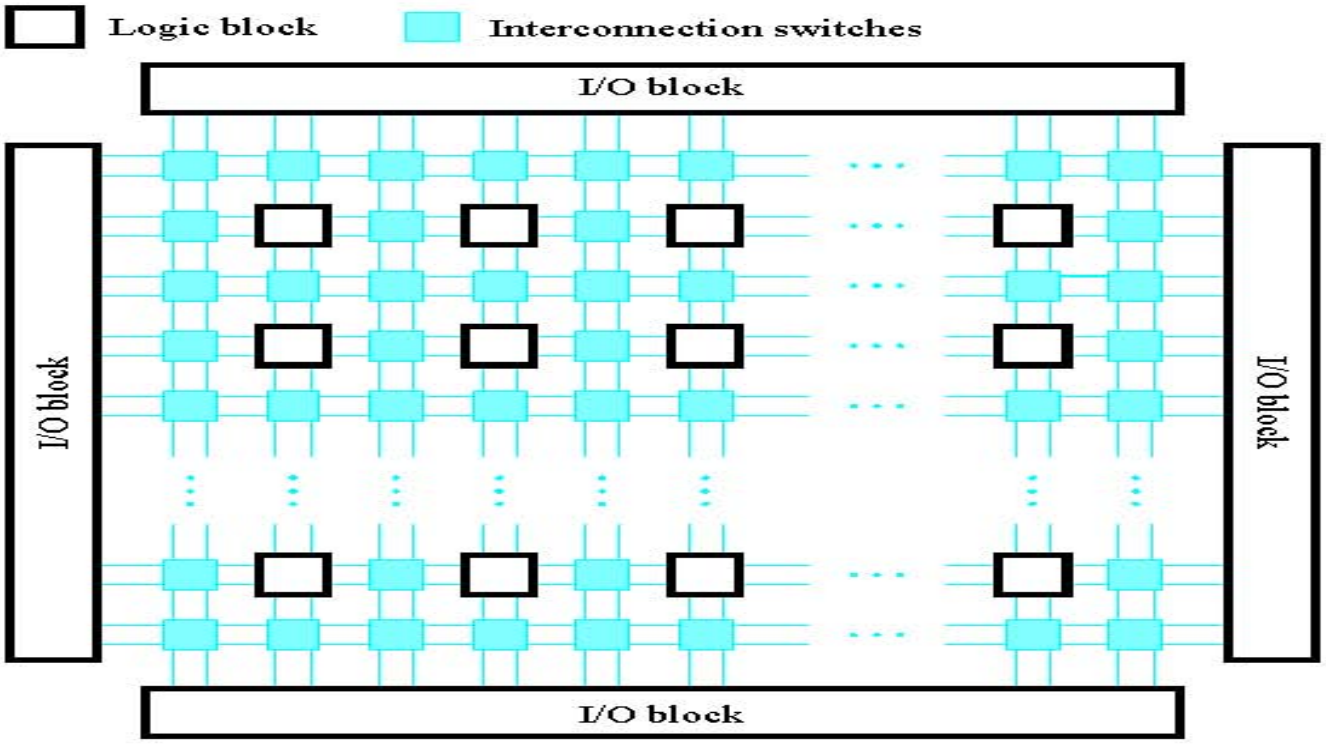


(a) CPLD in a Quad Flat Pack (QFP) package

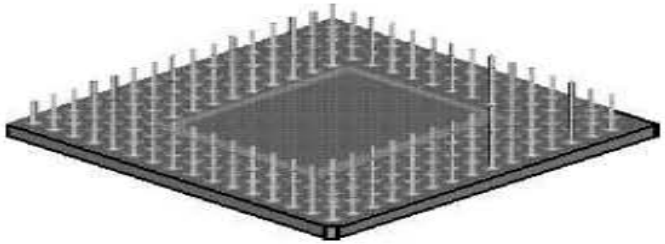


(b) JTAG programming

Figure 3.34. CPLD packaging and programming.

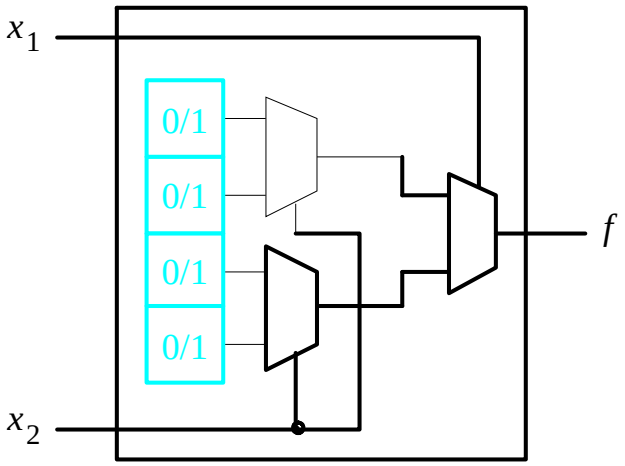


(a) General structure of an FPGA



(b) Pin grid array (PGA) package (bottom view)

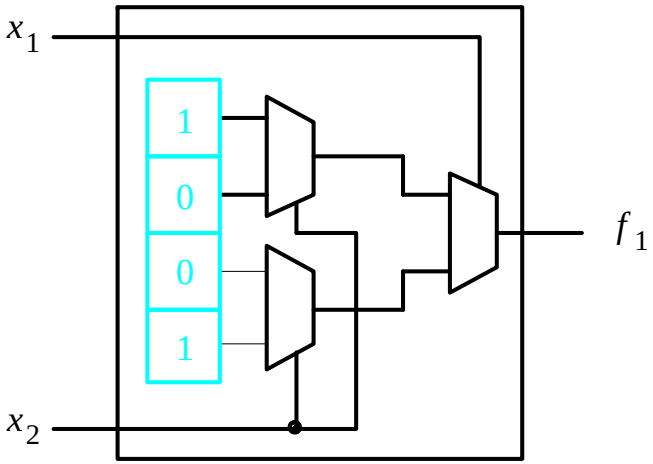
Figure 3.35. A field-programmable gate array (FPGA).



(a) Circuit for a two-input LUT

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$



(c) Storage cell contents in the LUT

Figure 3.36. A two-input lookup table (LUT).

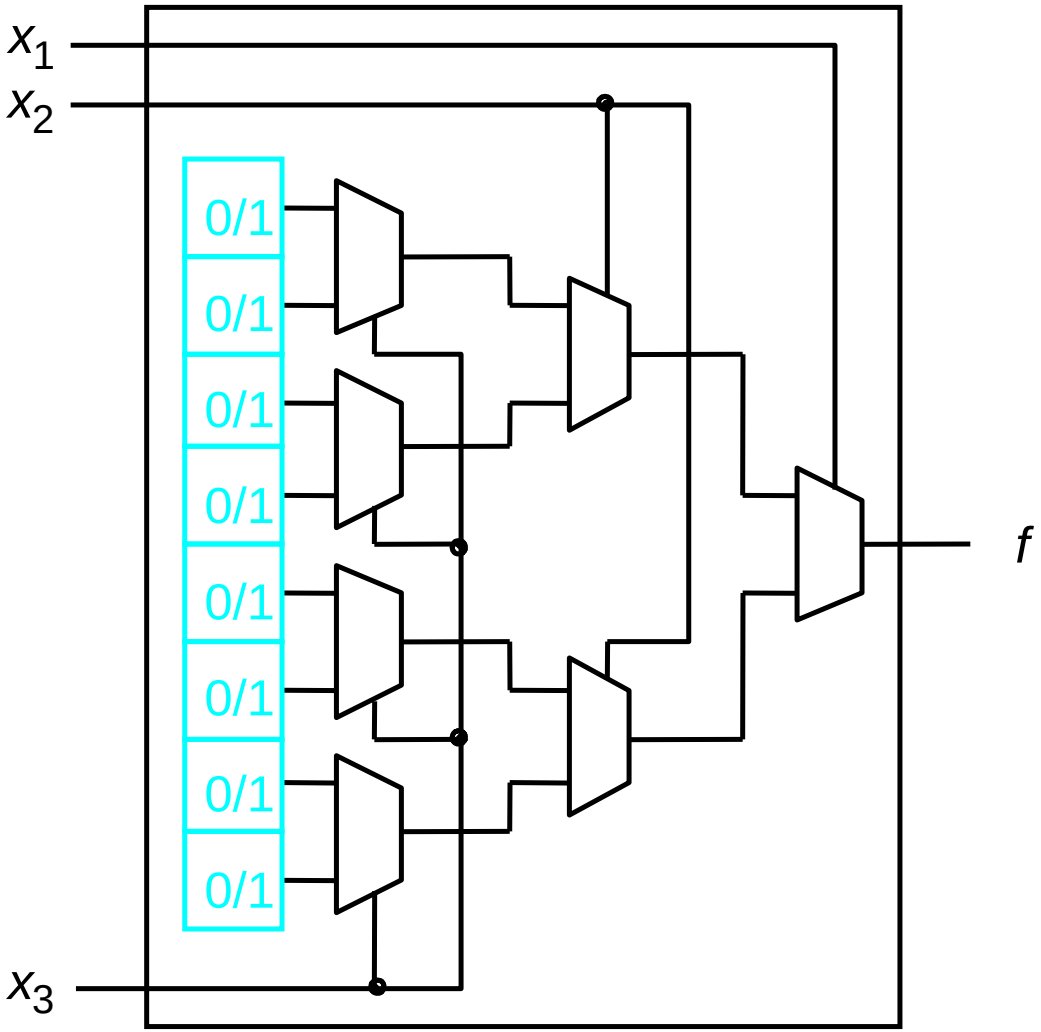


Figure 3.37. A three-input LUT.

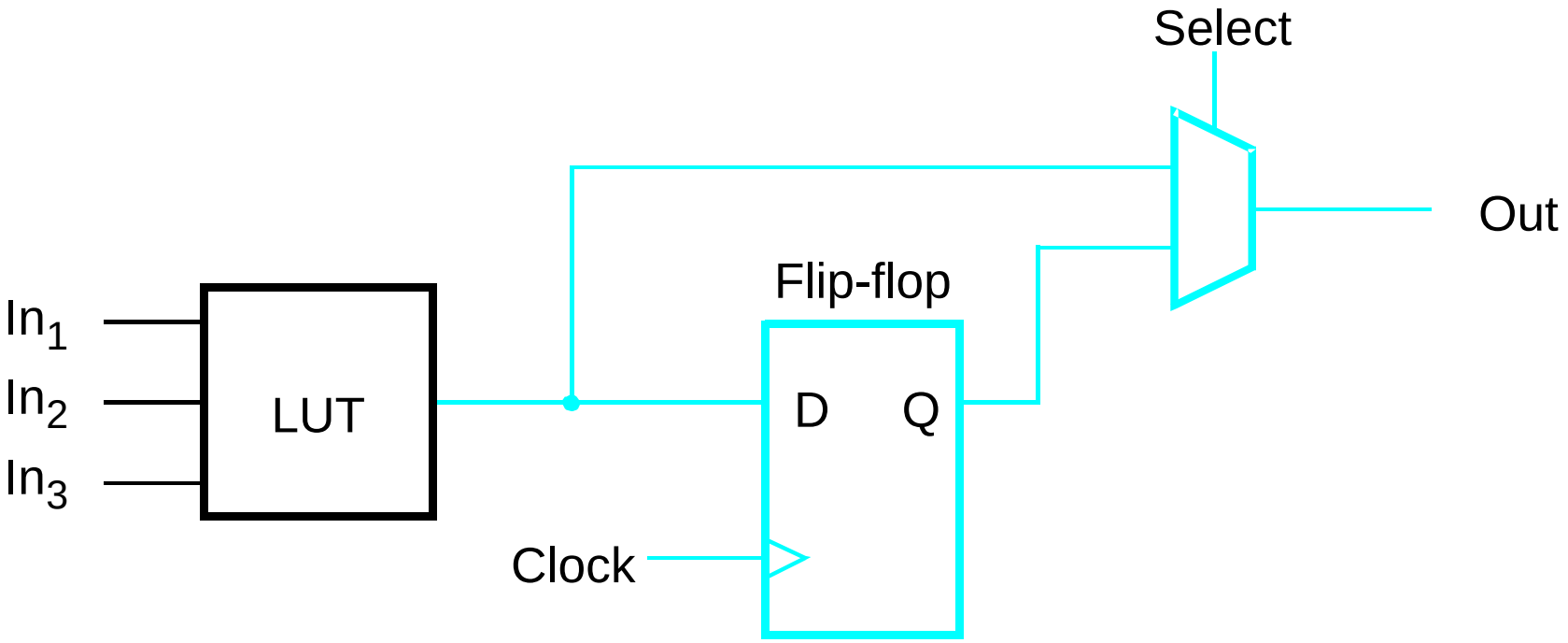


Figure 3.38. Inclusion of a flip-flop in an FPGA logic block.

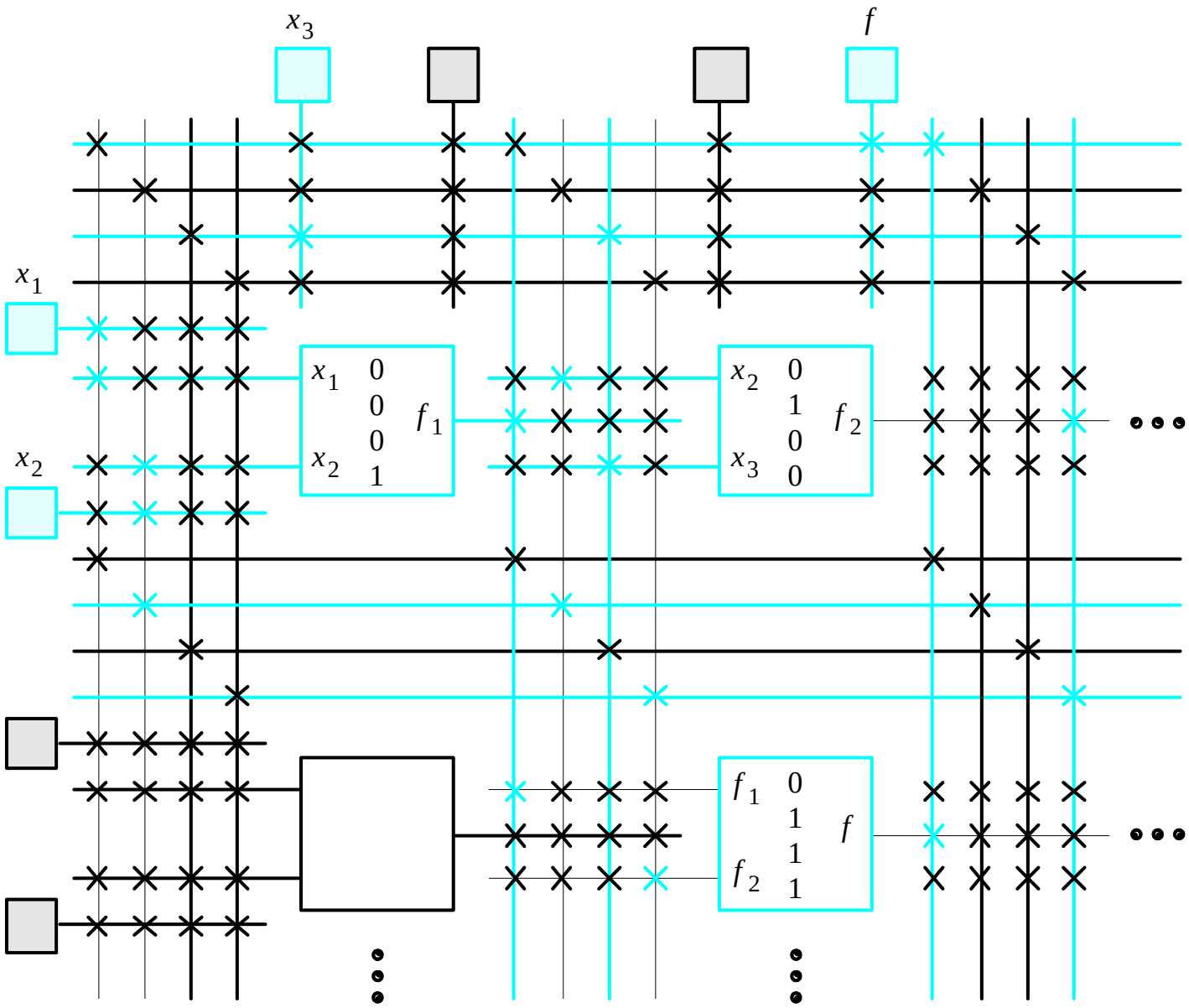


Figure 3.39. A section of a programmed FPGA.

CIs construídos a partir de Células Padrões: ASIC (Aplication Specific Integrated Circuit)

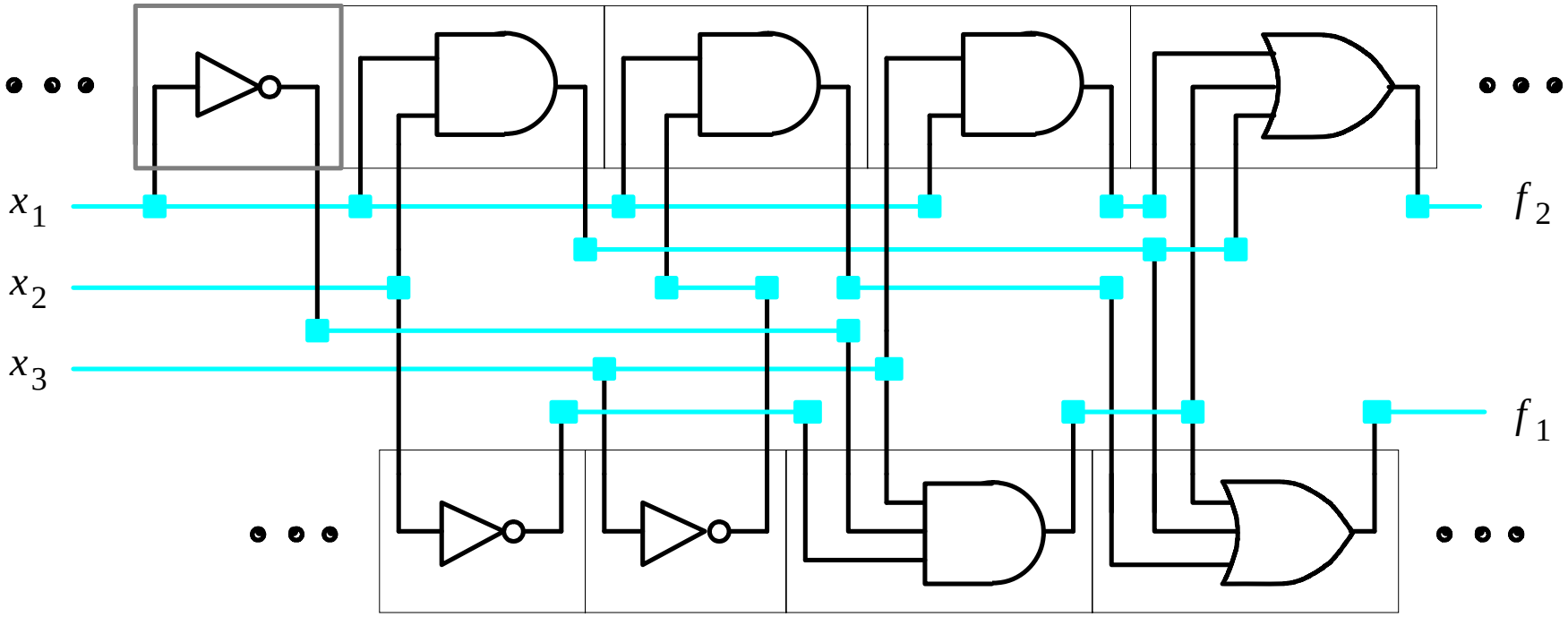


Figure 3.40. A section of two rows in a standard-cell chip

Matriz de portas lógicas:
nesse caso todas as células/portas são idênticas

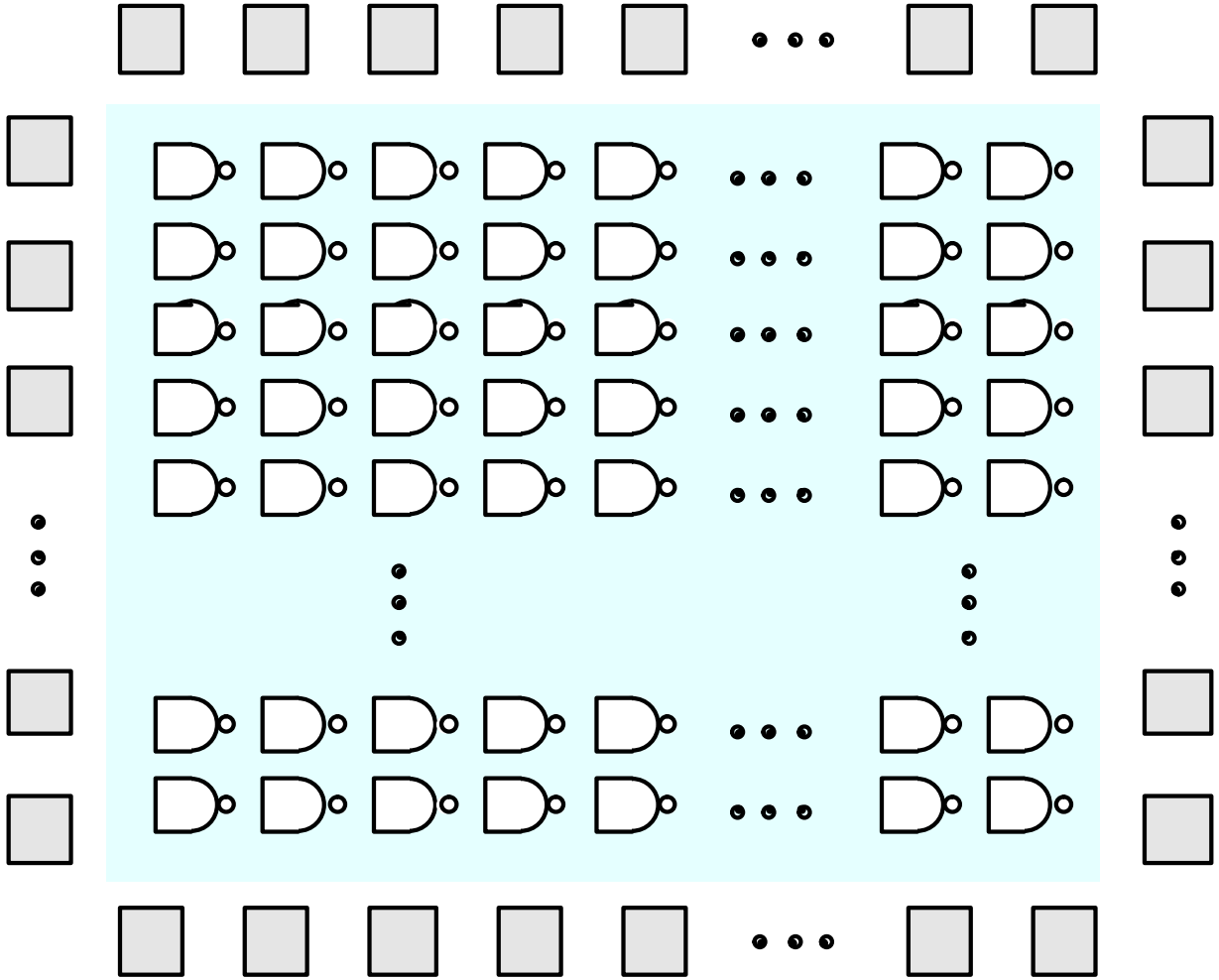


Figure 3.41. A sea-of-gates gate array.

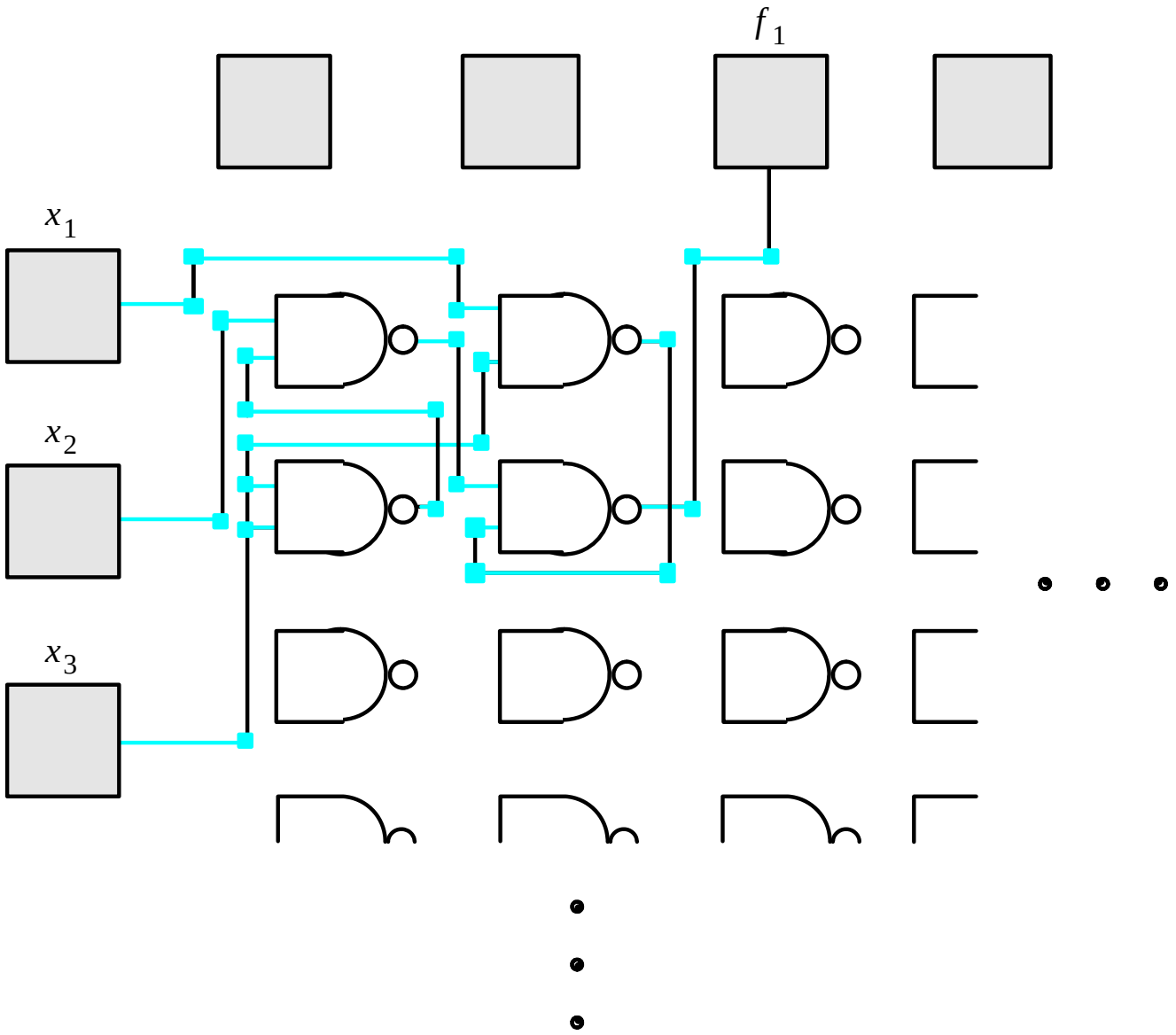
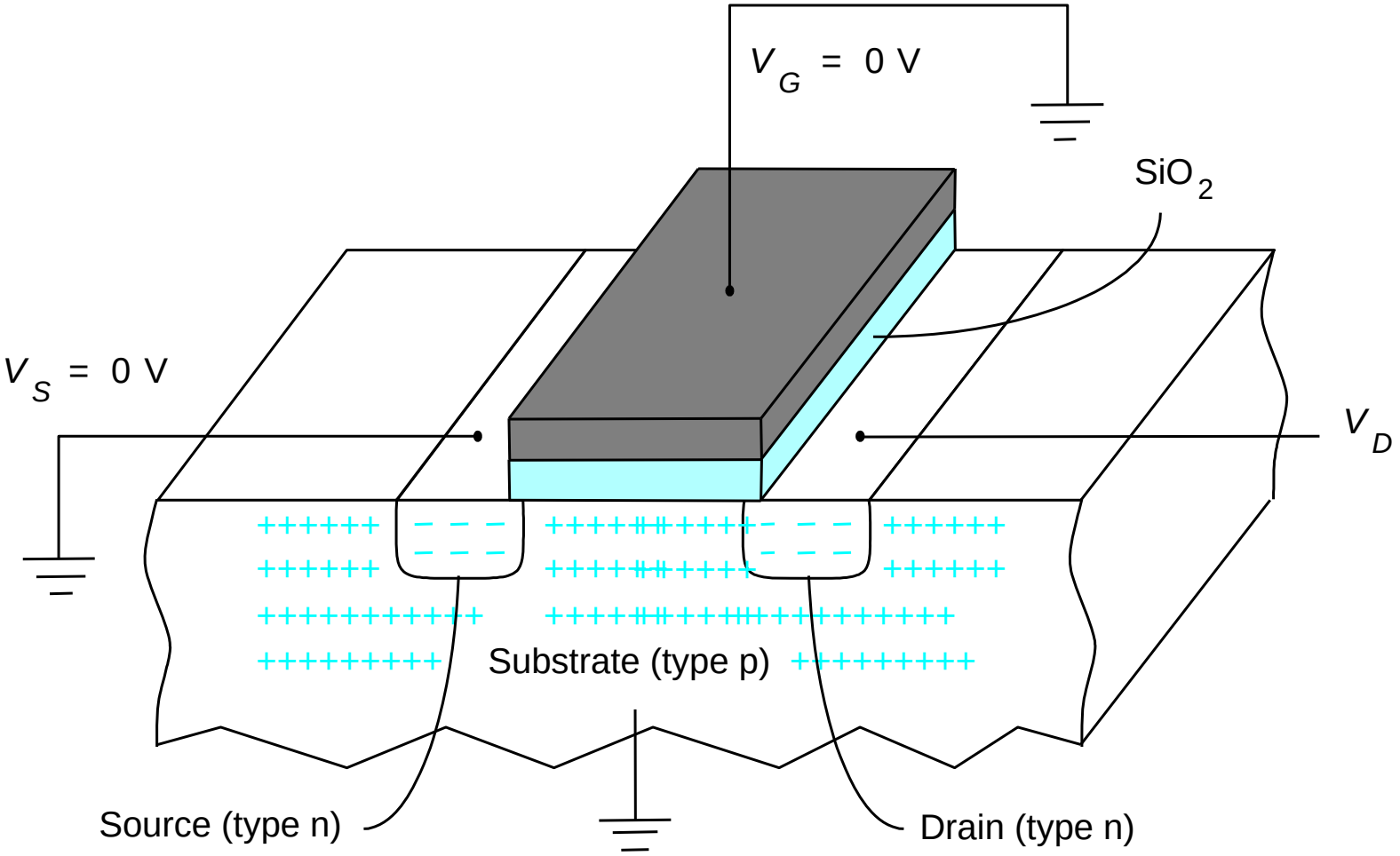


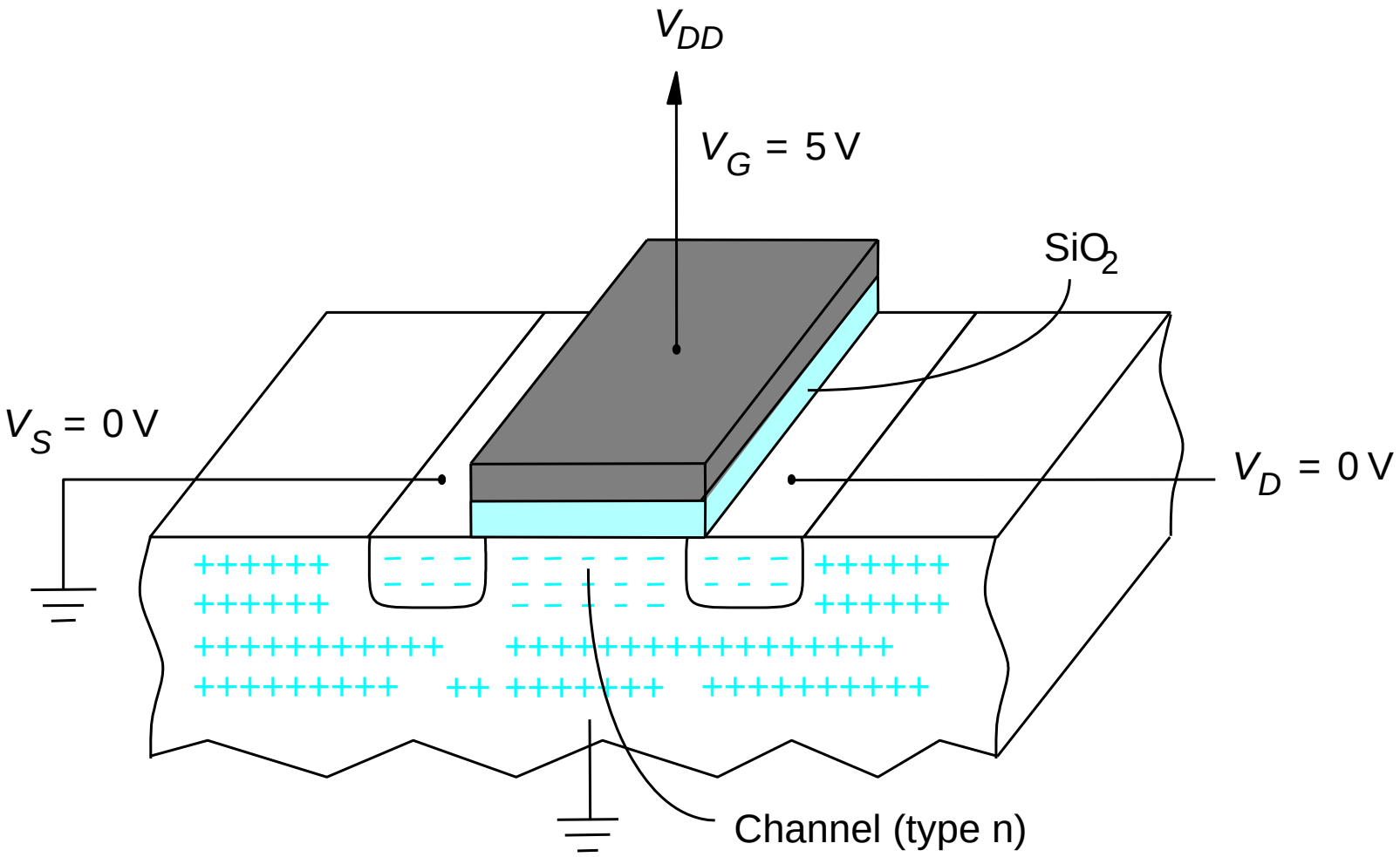
Figure 3.42. The logic function $f_1 = x_2\bar{x}_3 + x_1x_3$ in the gate array of Figure 3.41.

Estrutura física de um transistor do tipo MMOS



(a) When V_{GS} = 0 V, the transistor is off

Figure 3.43*a*. NMOS transistor when turned off.



(b) When V_{GS} = 5 V, the transistor is on

Figure 3.43*b*. NMOS transistor when turned on.

Fábrica Virtual de Circuito Integrado

- http://www.necel.com/v_factory/en/index.html