SCE 0110 -
Elementos de Lógica Digital I

Flip-Flops, Registradores e Contadores (continuacao)

Prof. Dr. Vanderlei Bonato

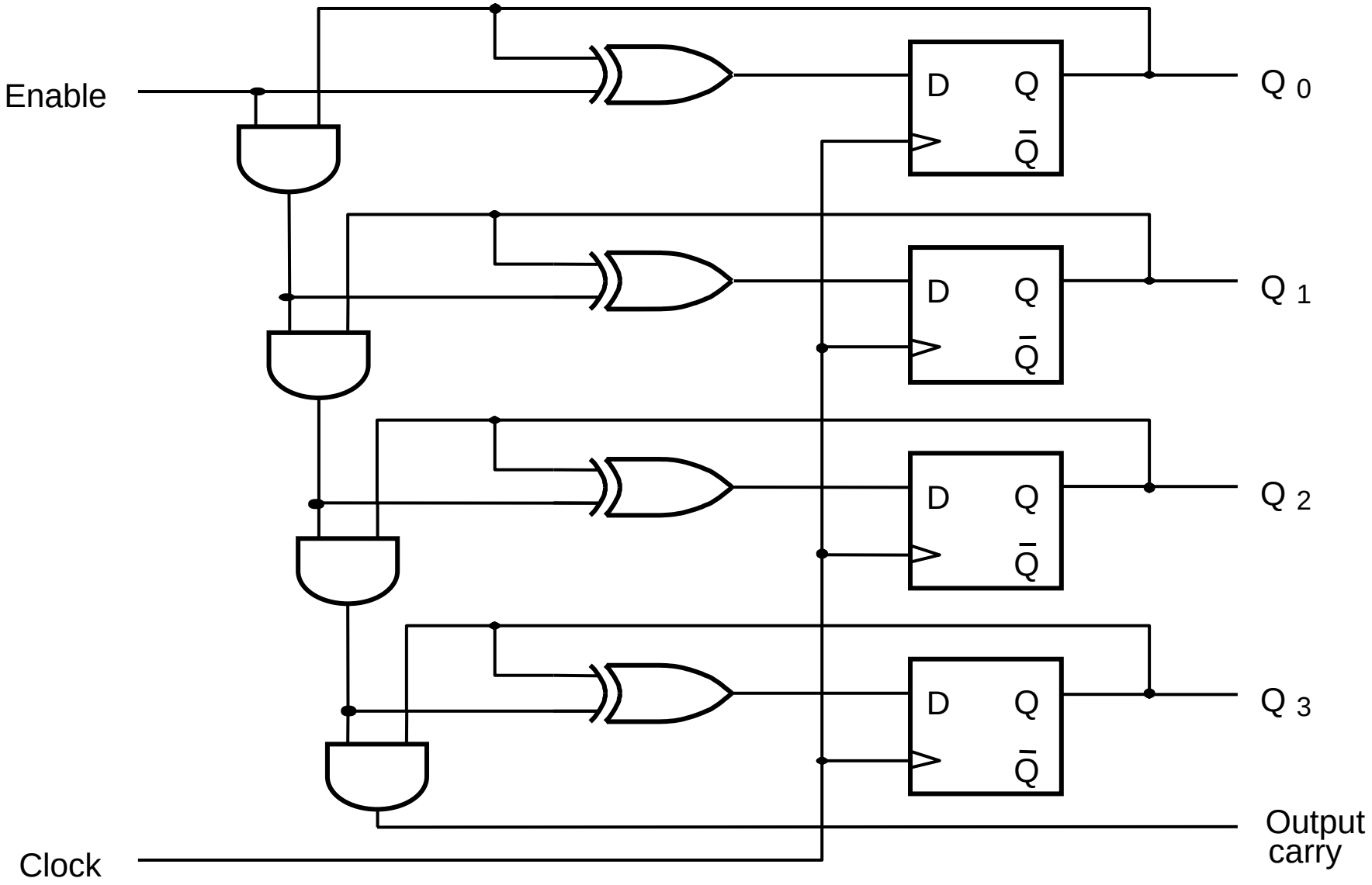


Figure 7.24. A four-bit counter with D flip-flops.

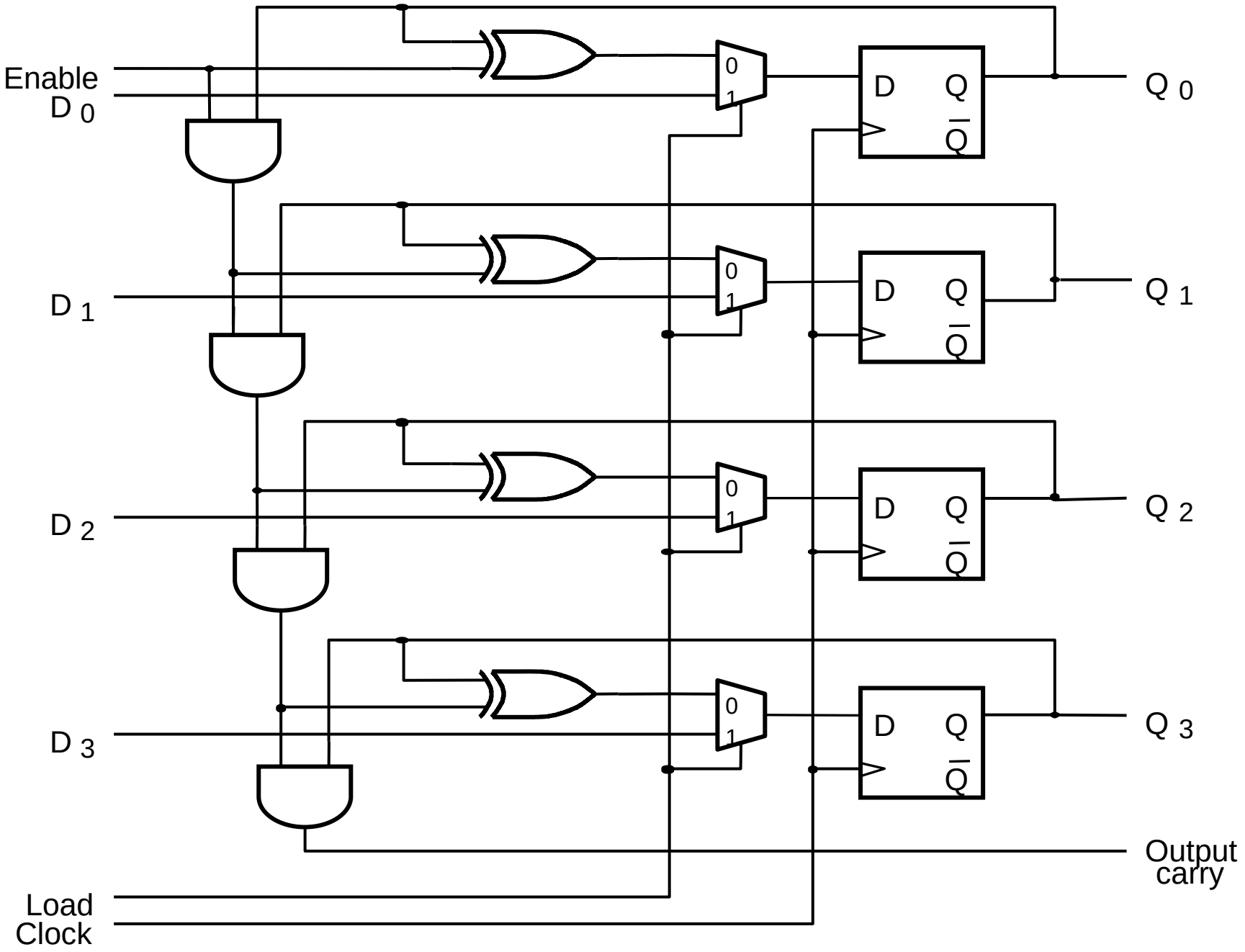


Figure 7.25. A counter with parallel-load capability.

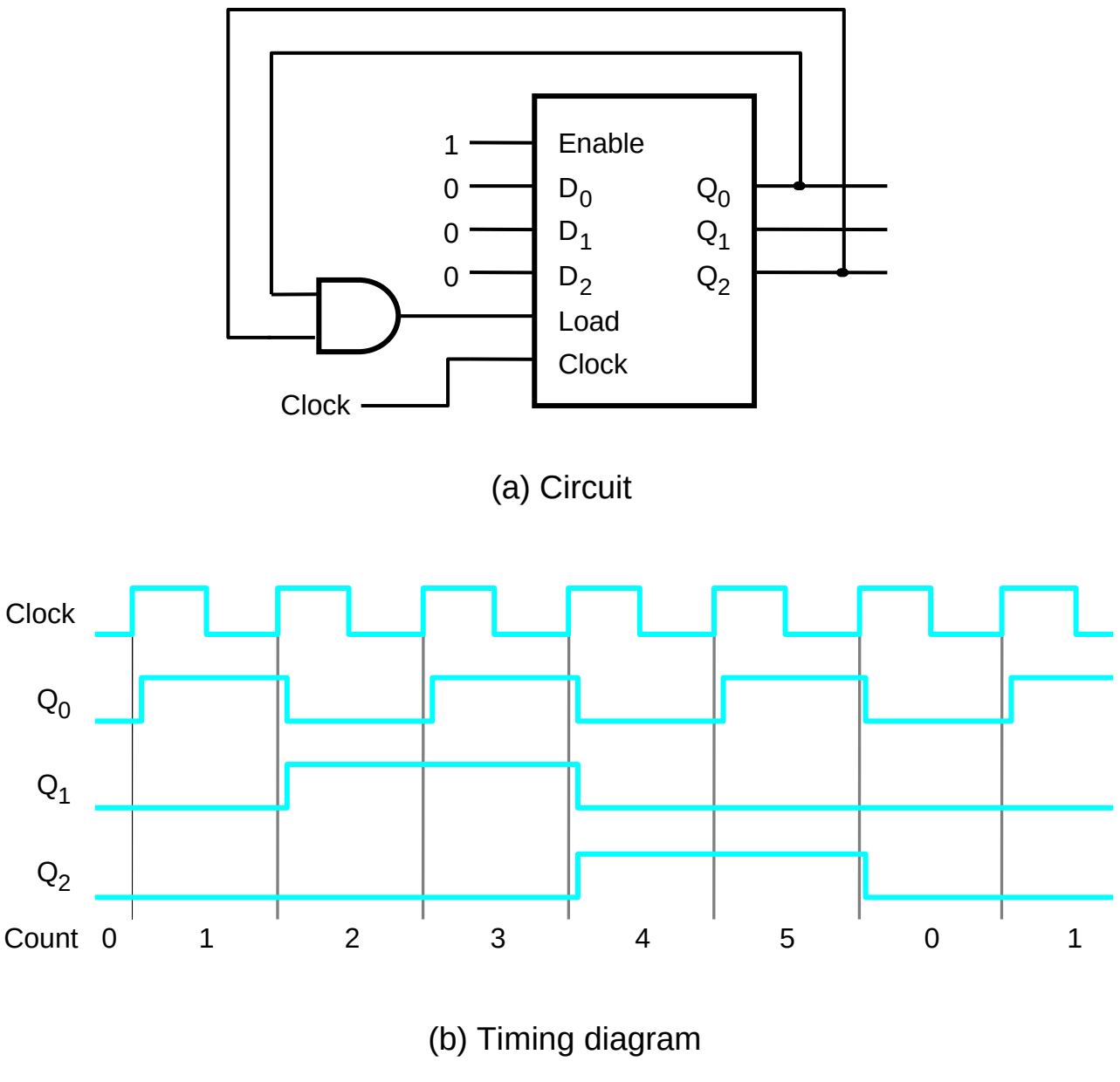


Figure 7.26. A modulo-6 counter with synchronous reset.

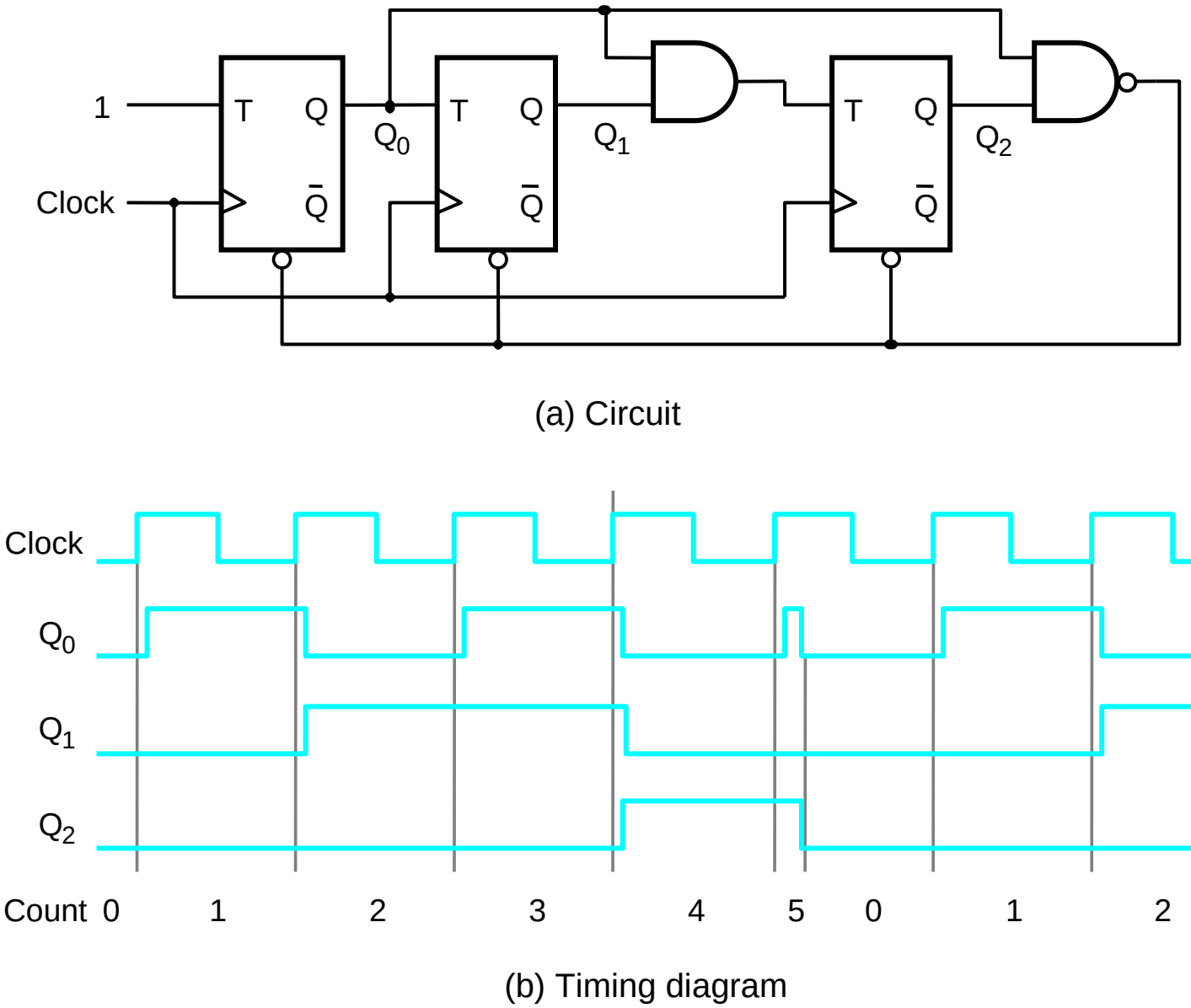


Figure 7.27. A modulo-6 counter with asynchronous reset.

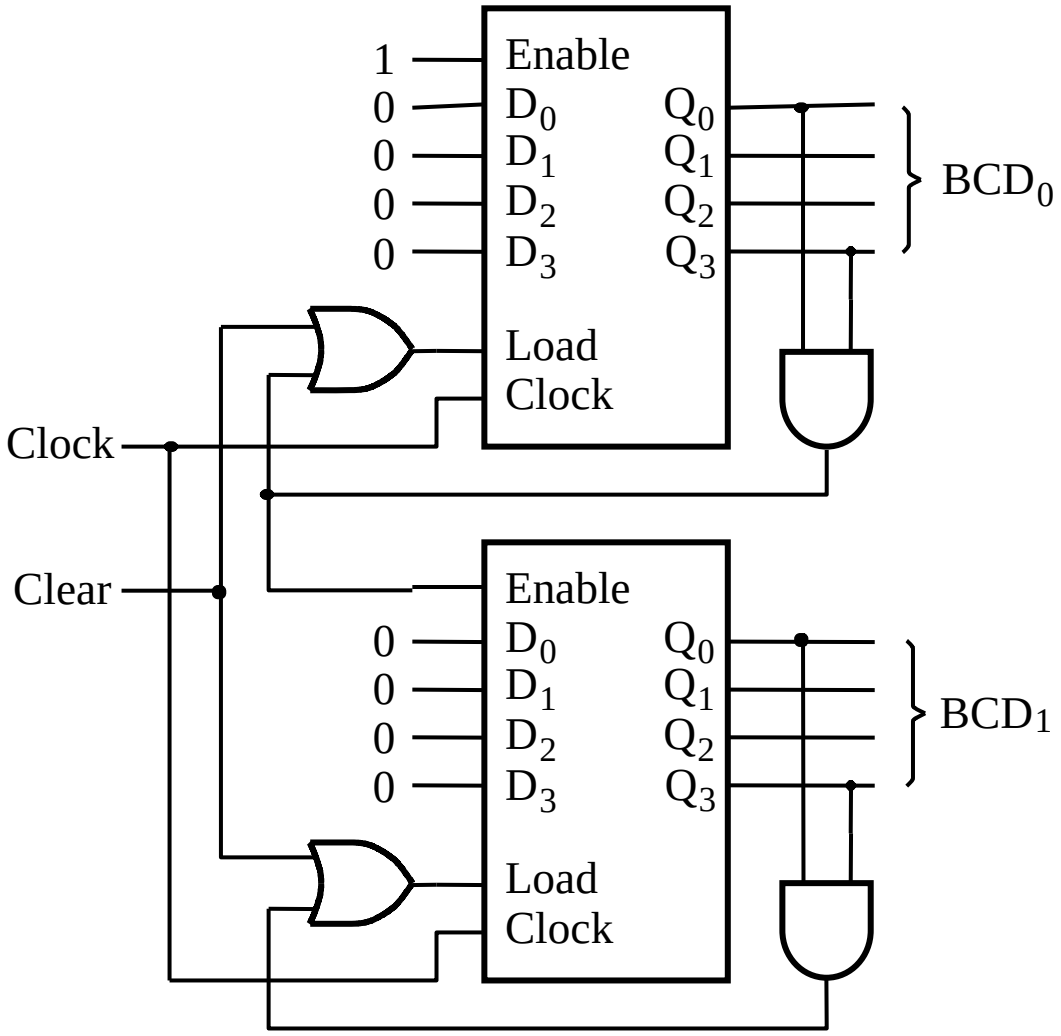
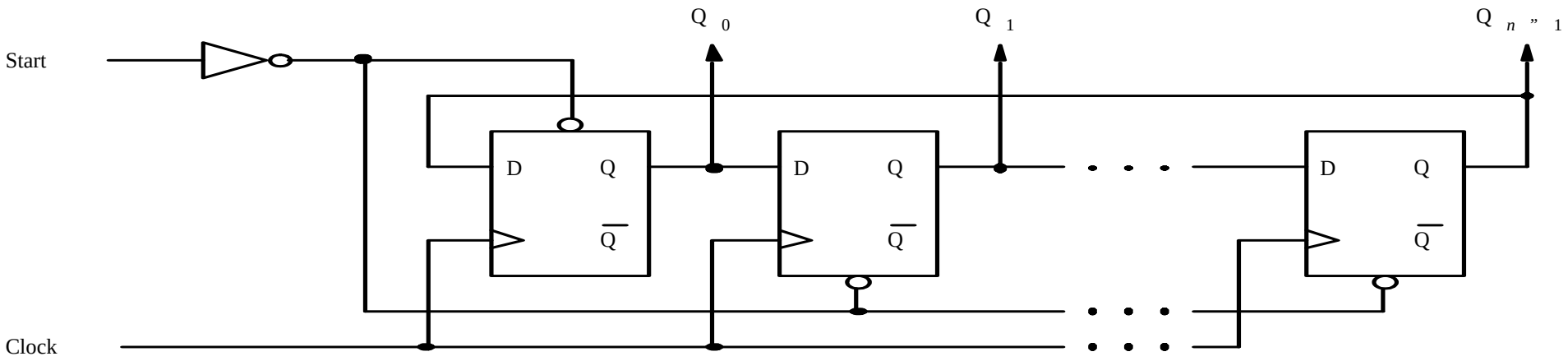
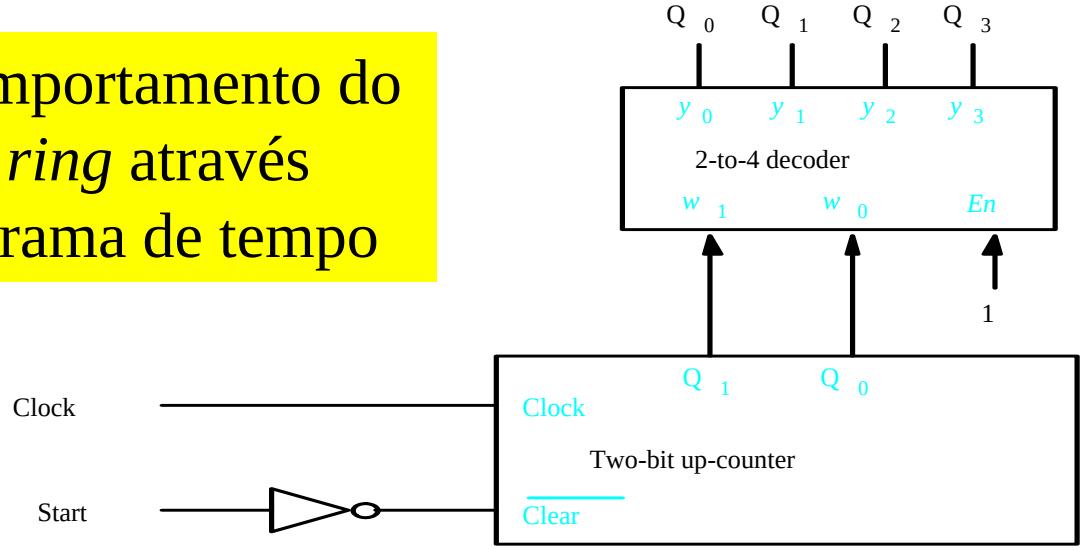


Figure 7.28. A two-digit BCD counter.



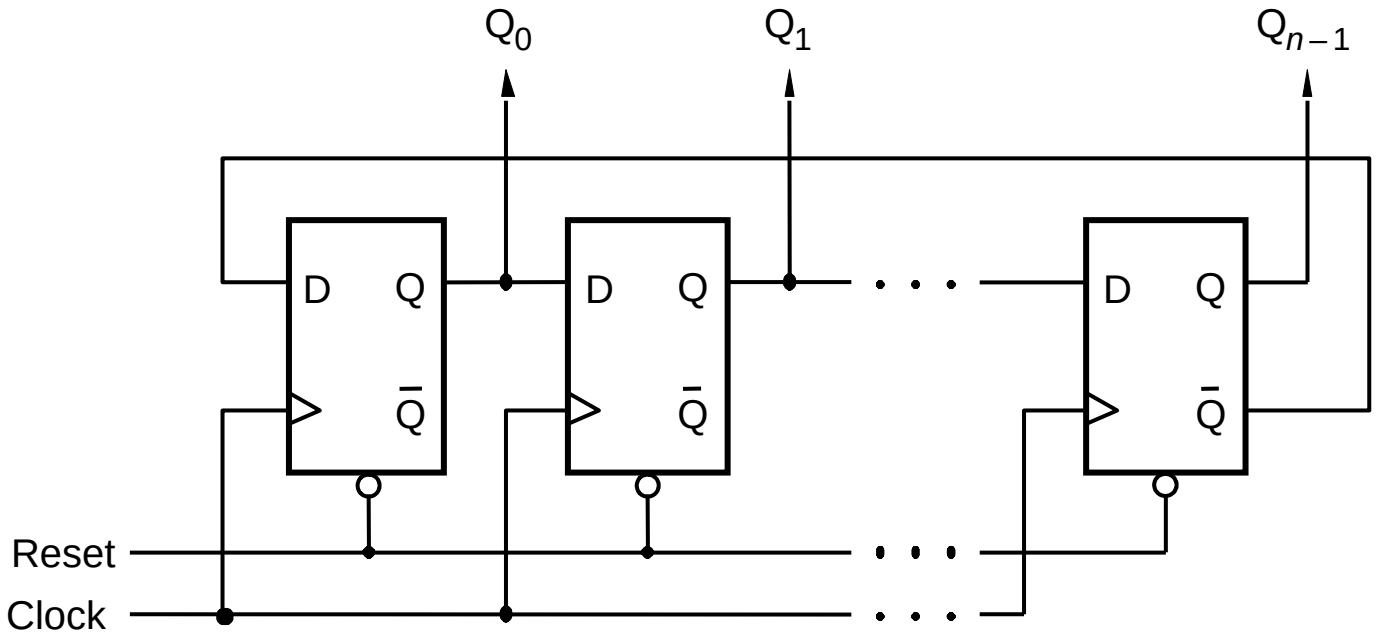
(a) An n -bit ring counter

Mostre o comportamento do contador *ring* através de um diagrama de tempo



(b) A four-bit ring counter

Figure 7.29. Ring counter.

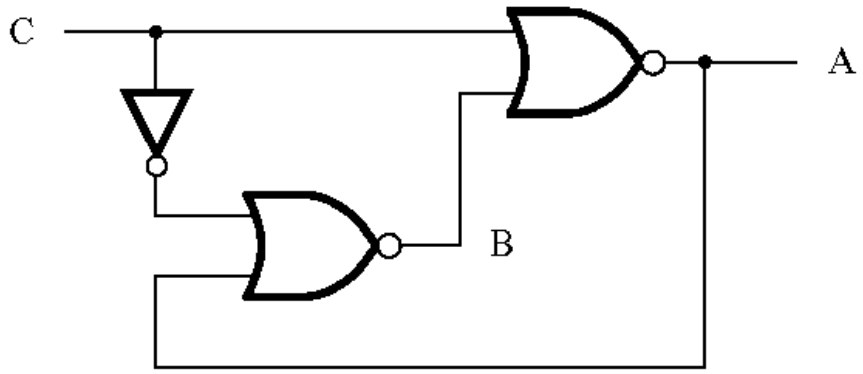


Mostre o comportamento do contador **Johnson** através de um diagrama de tempo

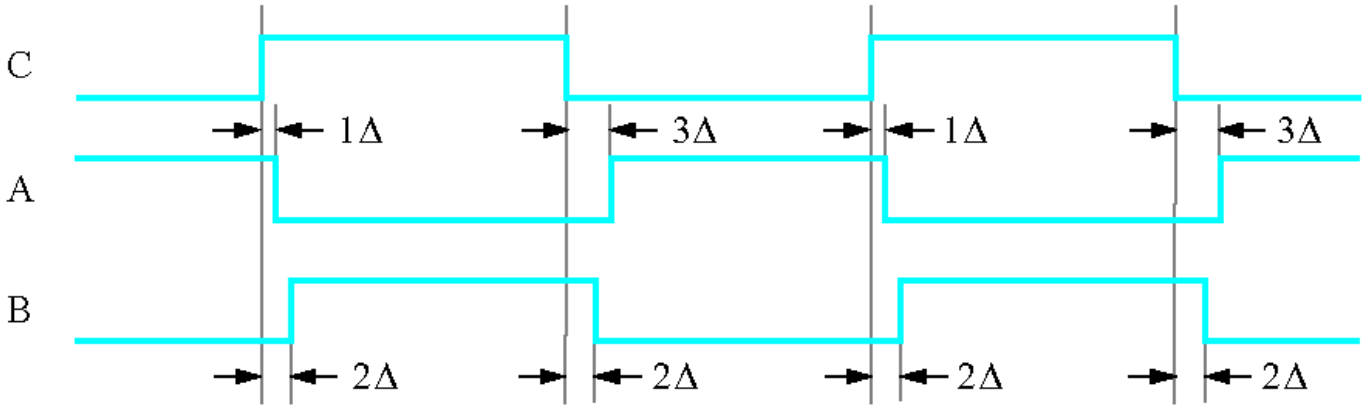
Figure 7.30. Johnson counter.

Exercícios

- Mostre como obter um FF-D e um FF-T a partir de um FF-JK
- Estudar as questões relacionadas as respostas dos slides seguintes



(a) Circuit



(b) Timing diagram

Figure 7.80. Circuit for Example 7.13.

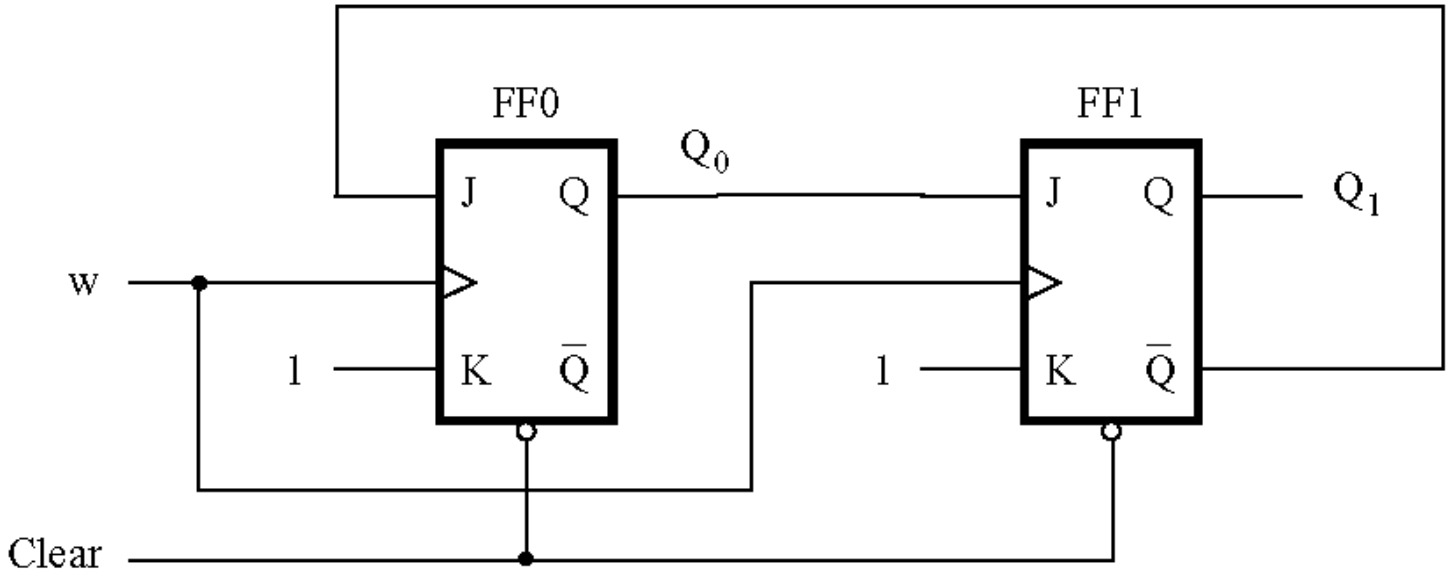


Figure 7.81. Circuit for Example 7.14.

Time interval	FF0			FF1		
	J_0	K_0	Q_0	J_1	K_1	Q_1
Clear	1	1	0	0	1	0
t_1	1	1	1	1	1	0
t_2	0	1	0	0	1	1
t_3	1	1	0	0	1	0
t_4	1	1	1	1	1	0

Figure 7.82. Summary of the behavior of the circuit in Figure 7.81.

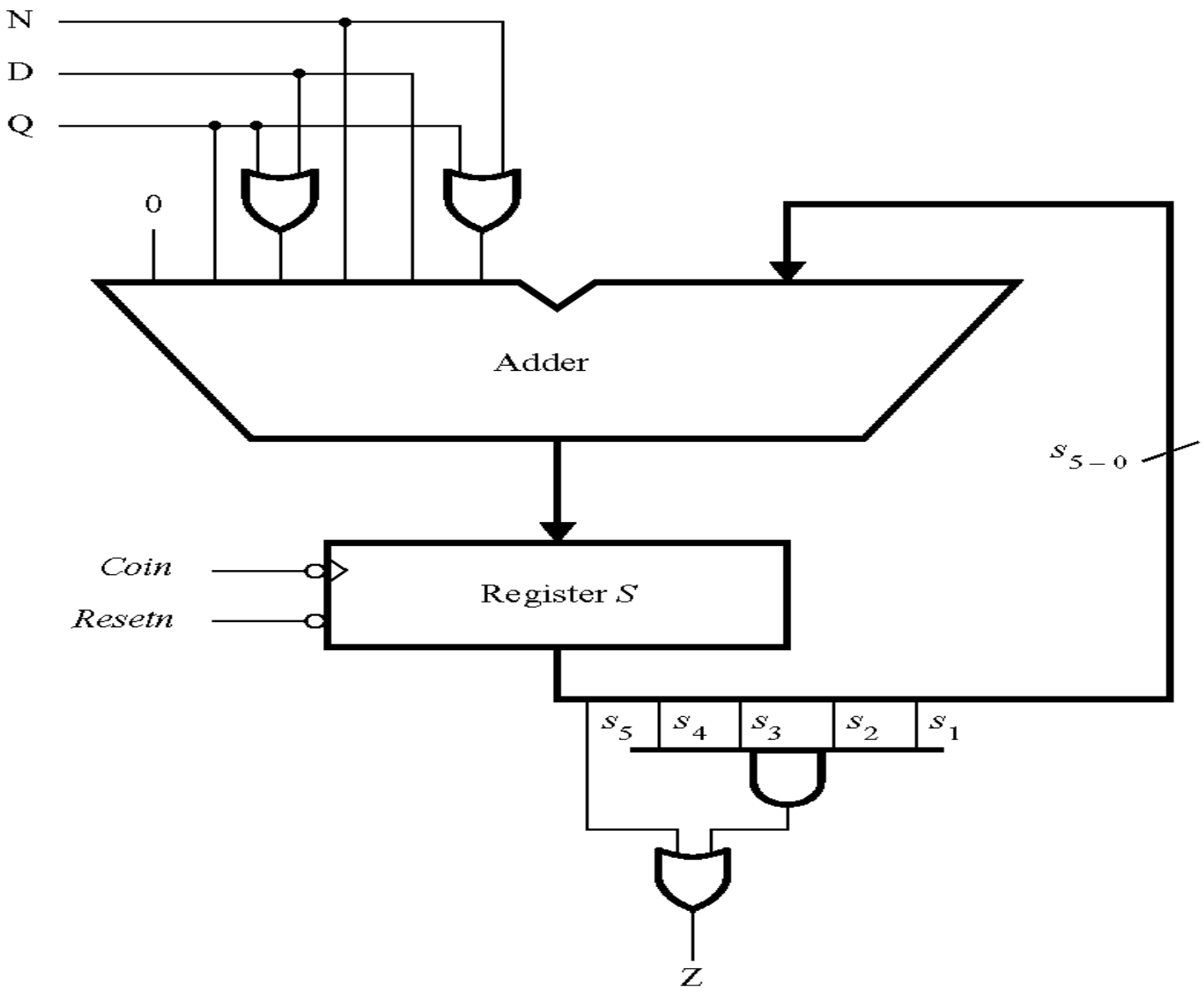


Figure 7.84. Circuit for Example 7.16.

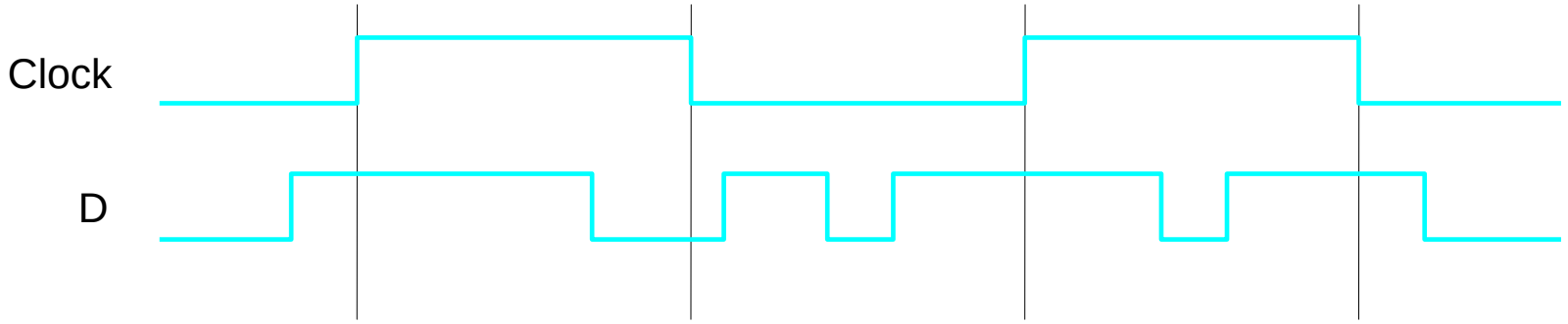


Figure P7.1. Timing diagram for problem 7.1.

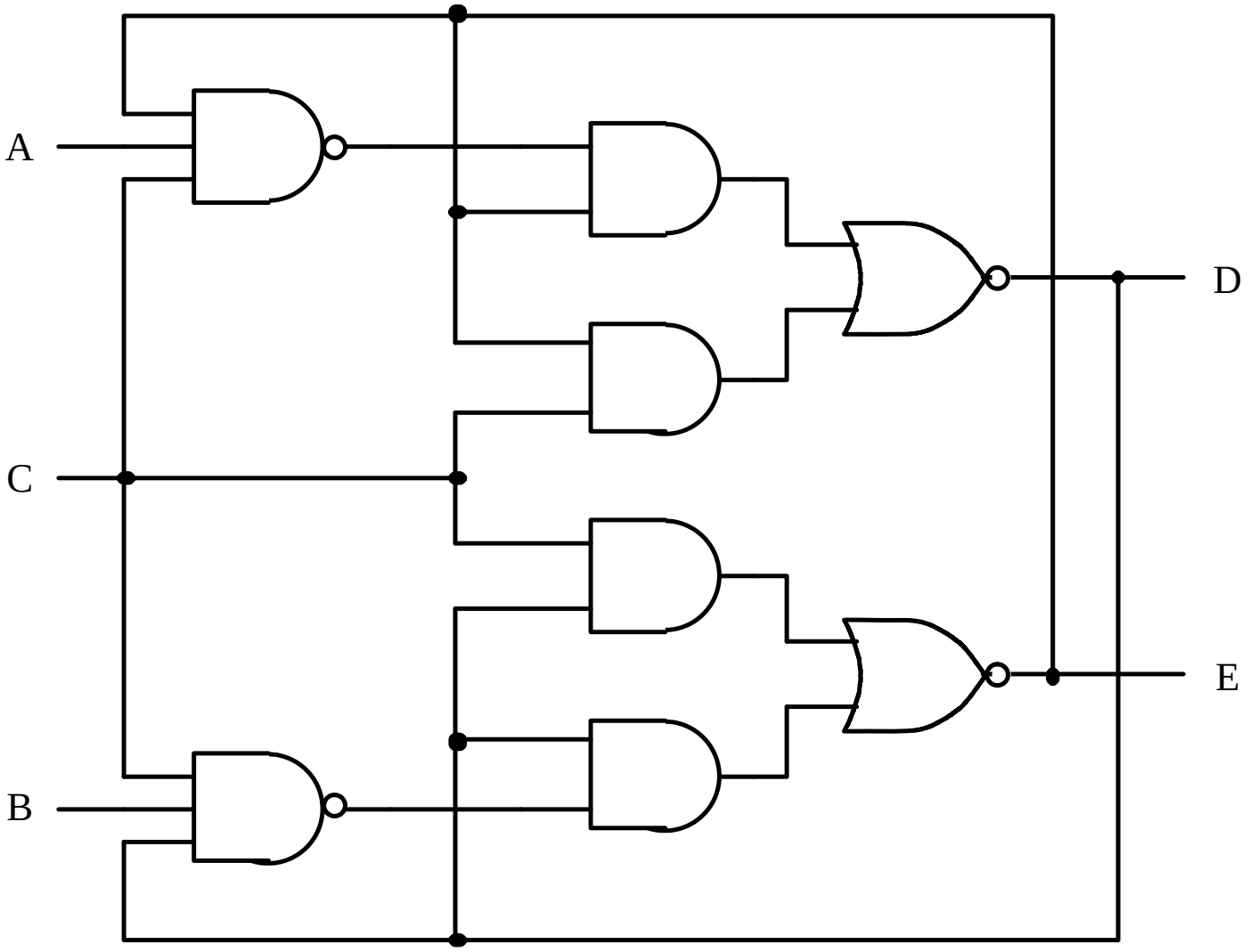


Figure P7.2. Circuit for problem 7.9.

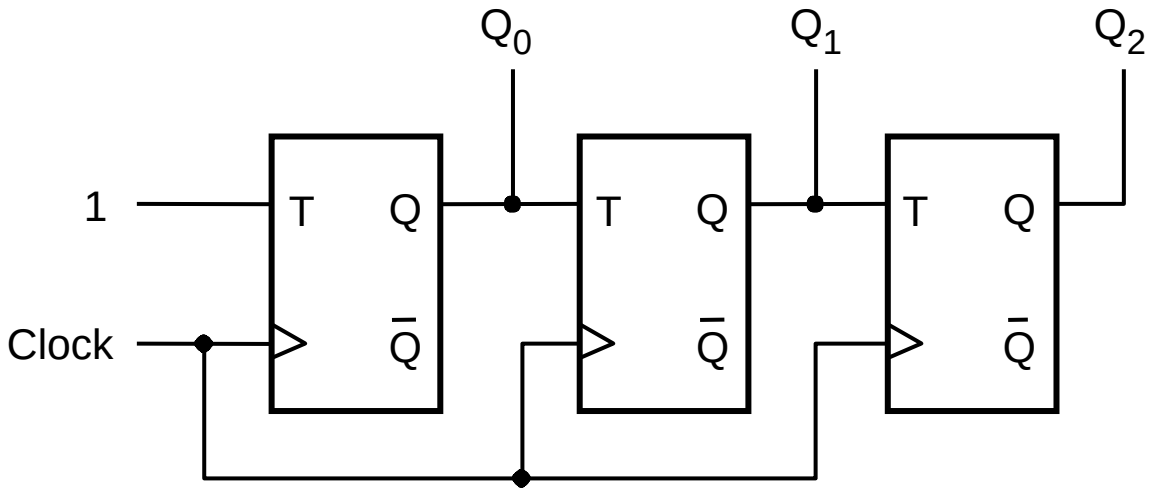


Figure P7.3. The circuit for problem 7.18.

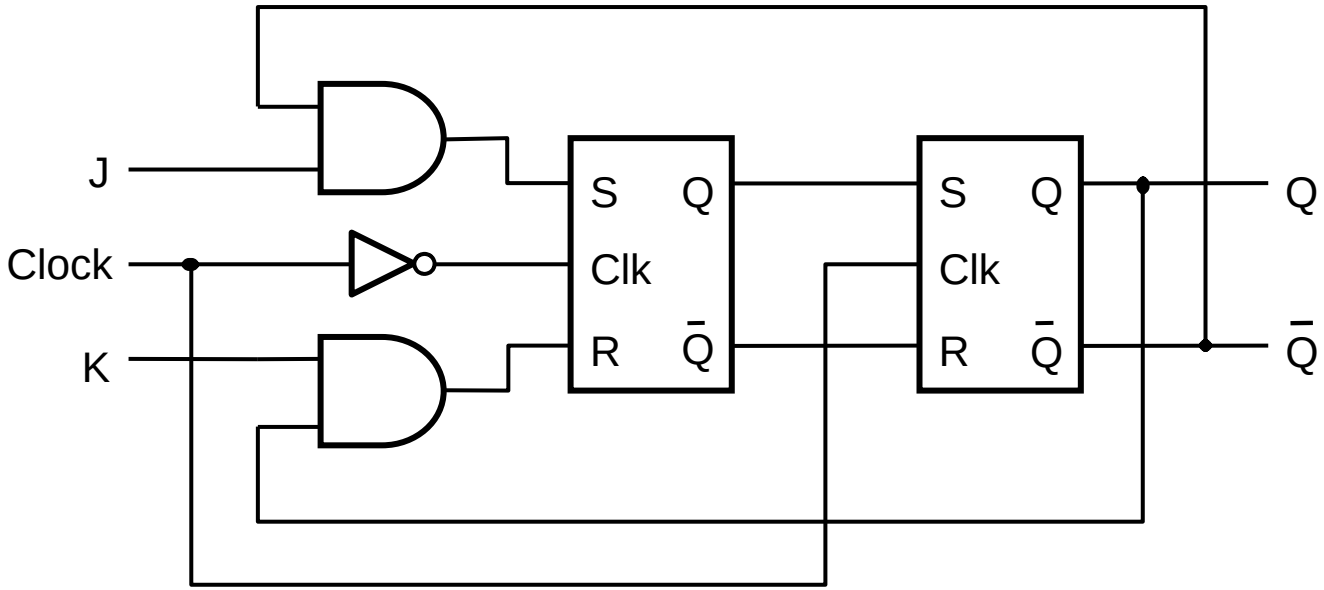


Figure P7.4. Circuit for problem 7.19.

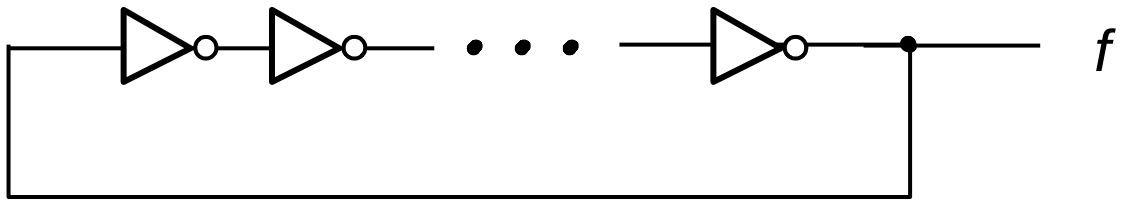


Figure P7.5. A ring oscillator.

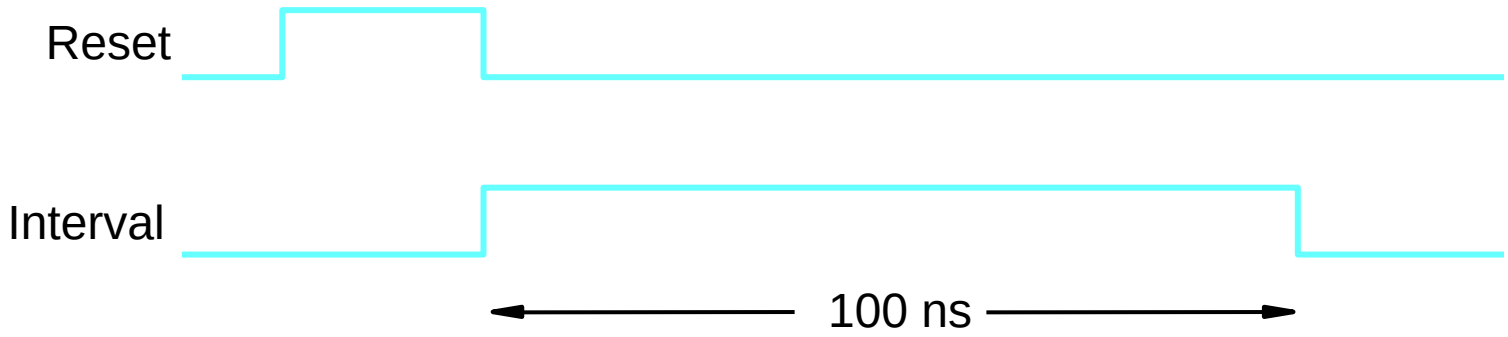


Figure P7.6. Timing of signals for problem 7.31.

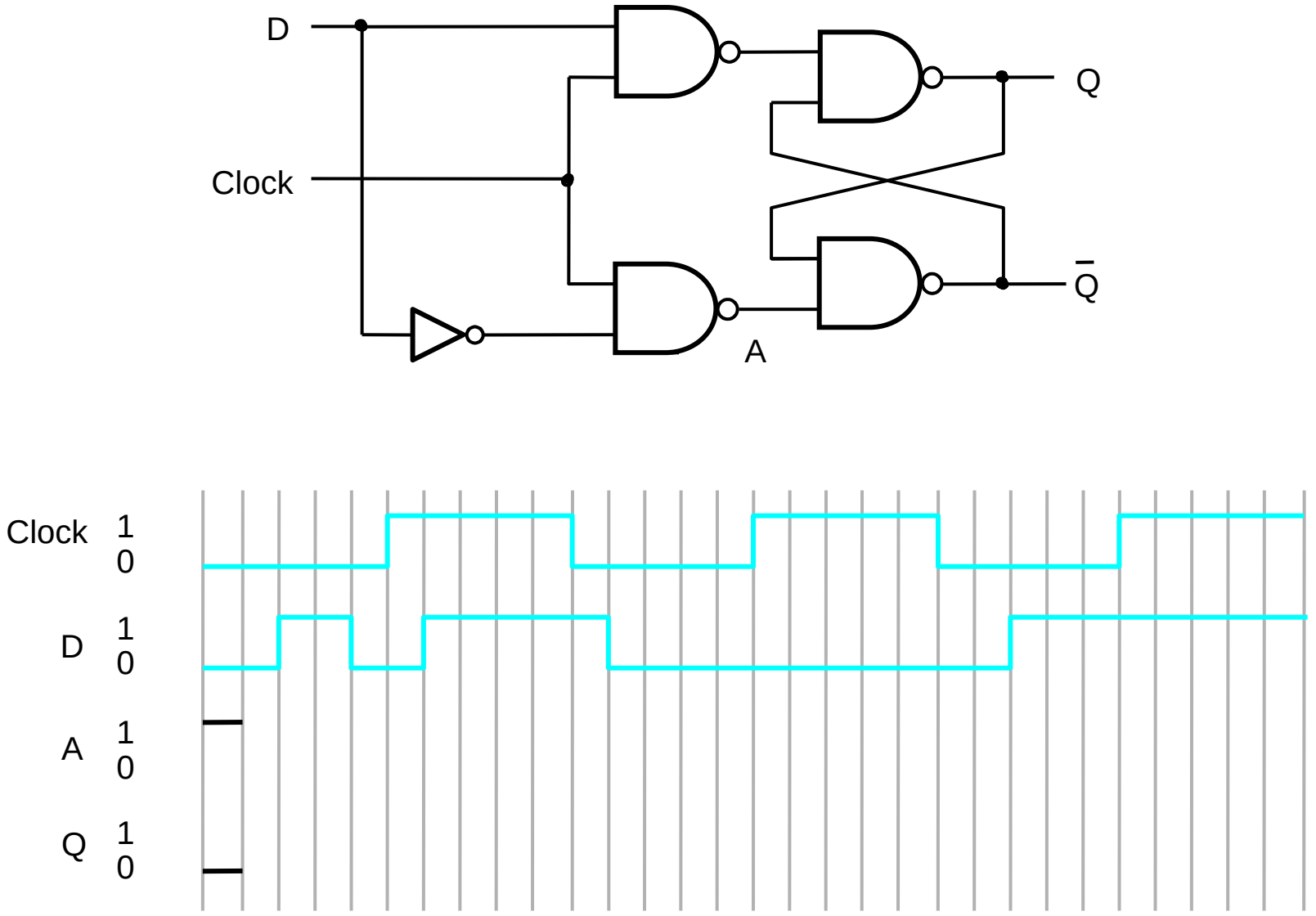


Figure P7.7. Circuit and timing diagram for problem 7.32.

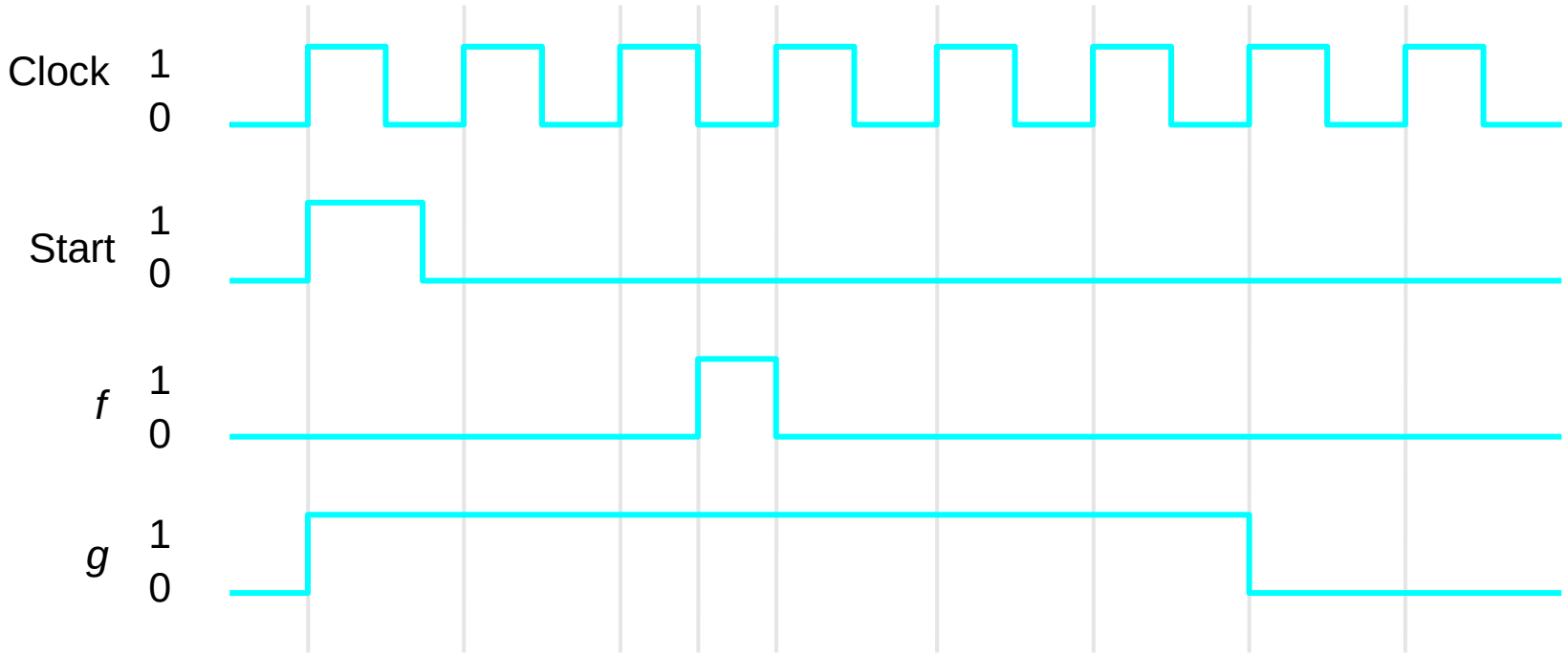


Figure P7.8. Timing diagram for problem 7.33.