SCE 0110 -
Elementos de Lógica Digital I

Flip-Flops, Registradores e Contadores (continuação)

Prof. Dr. Vanderlei Bonato

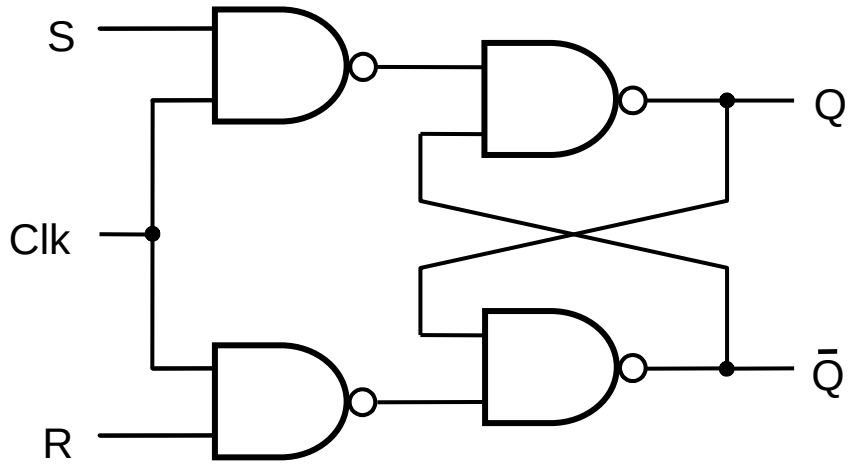
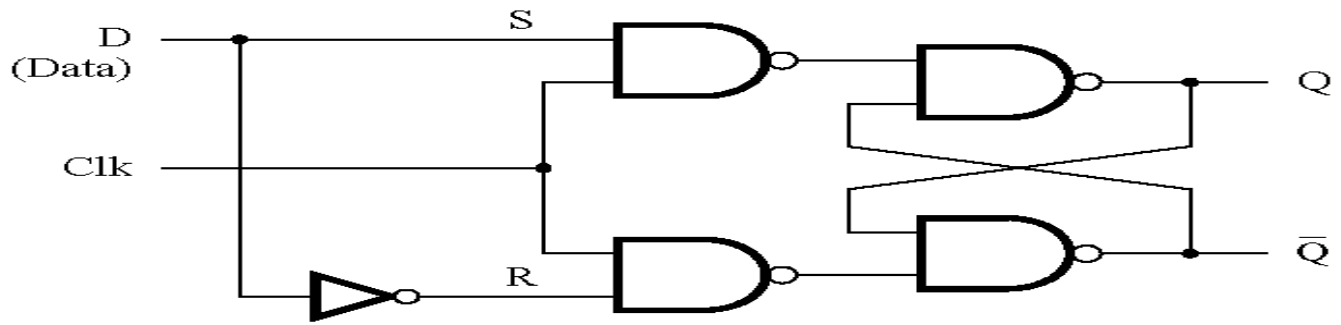


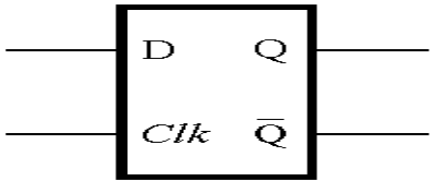
Figure 7.7. Gated SR latch with NAND gates.



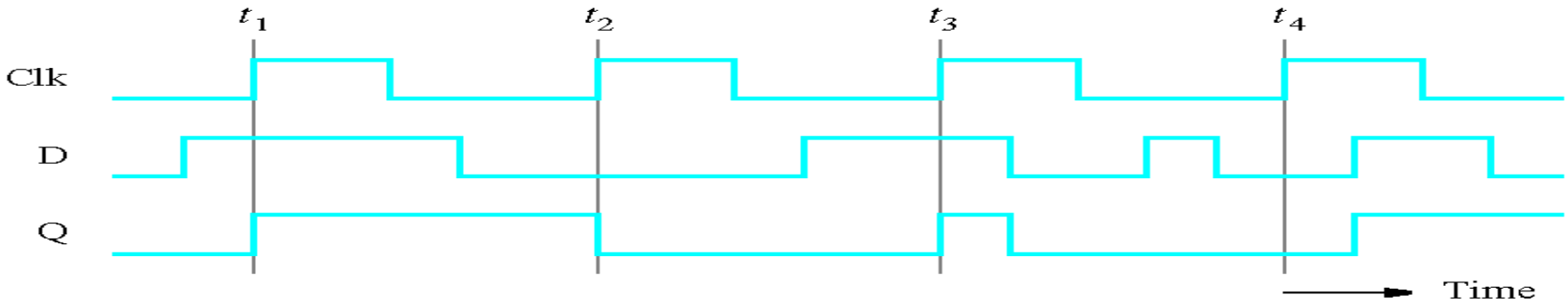
(a) Circuit

Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

(b) Characteristic table



(c) Graphical symbol



(d) Timing diagram

Figure 7.8. Gated D latch.

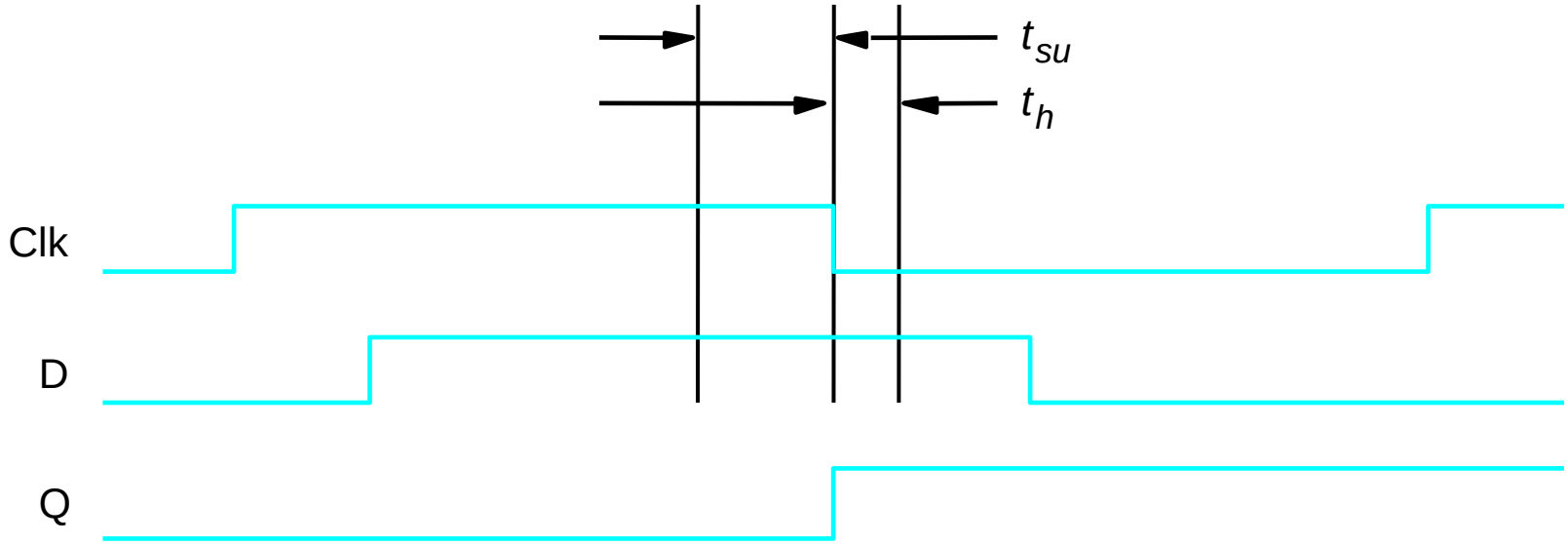
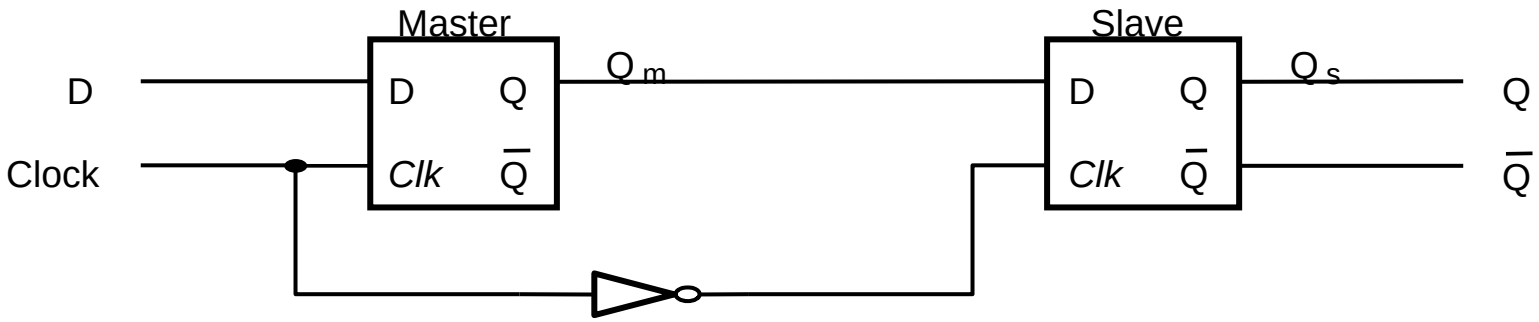
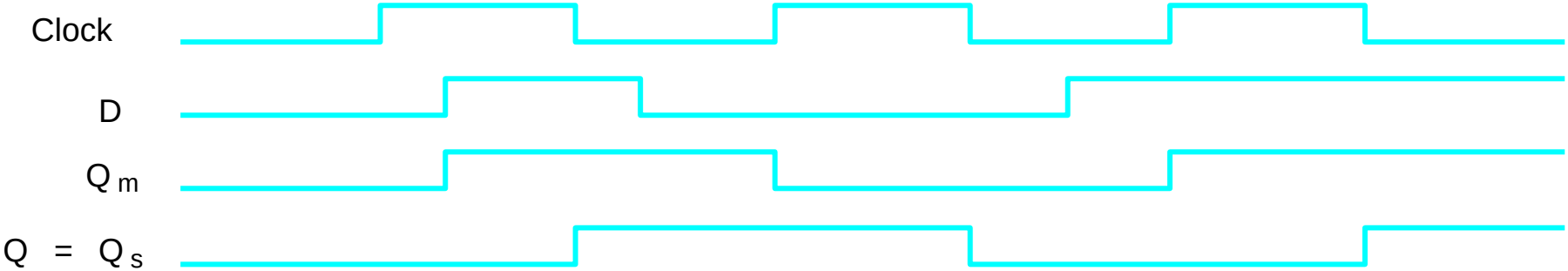


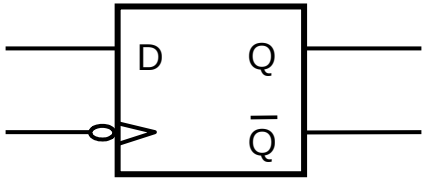
Figure 7.9. Setup and hold times.



(a) Circuit

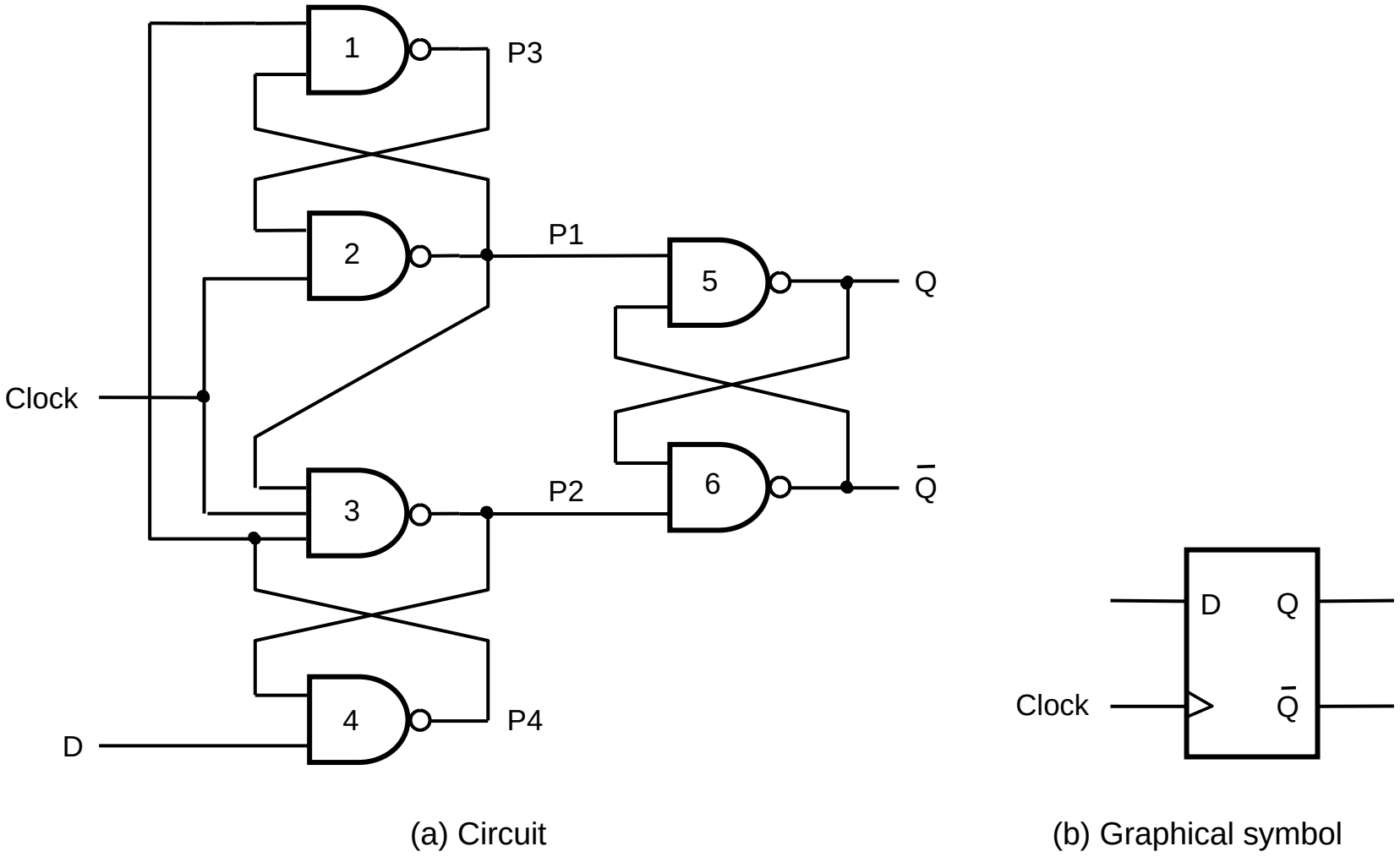


(b) Timing diagram



(c) Graphical symbol

Figure 7.10. Master-slave D flip-flop.



(a) Circuit

(b) Graphical symbol

Figure 7.11. A positive-edge-triggered D flip-flop.

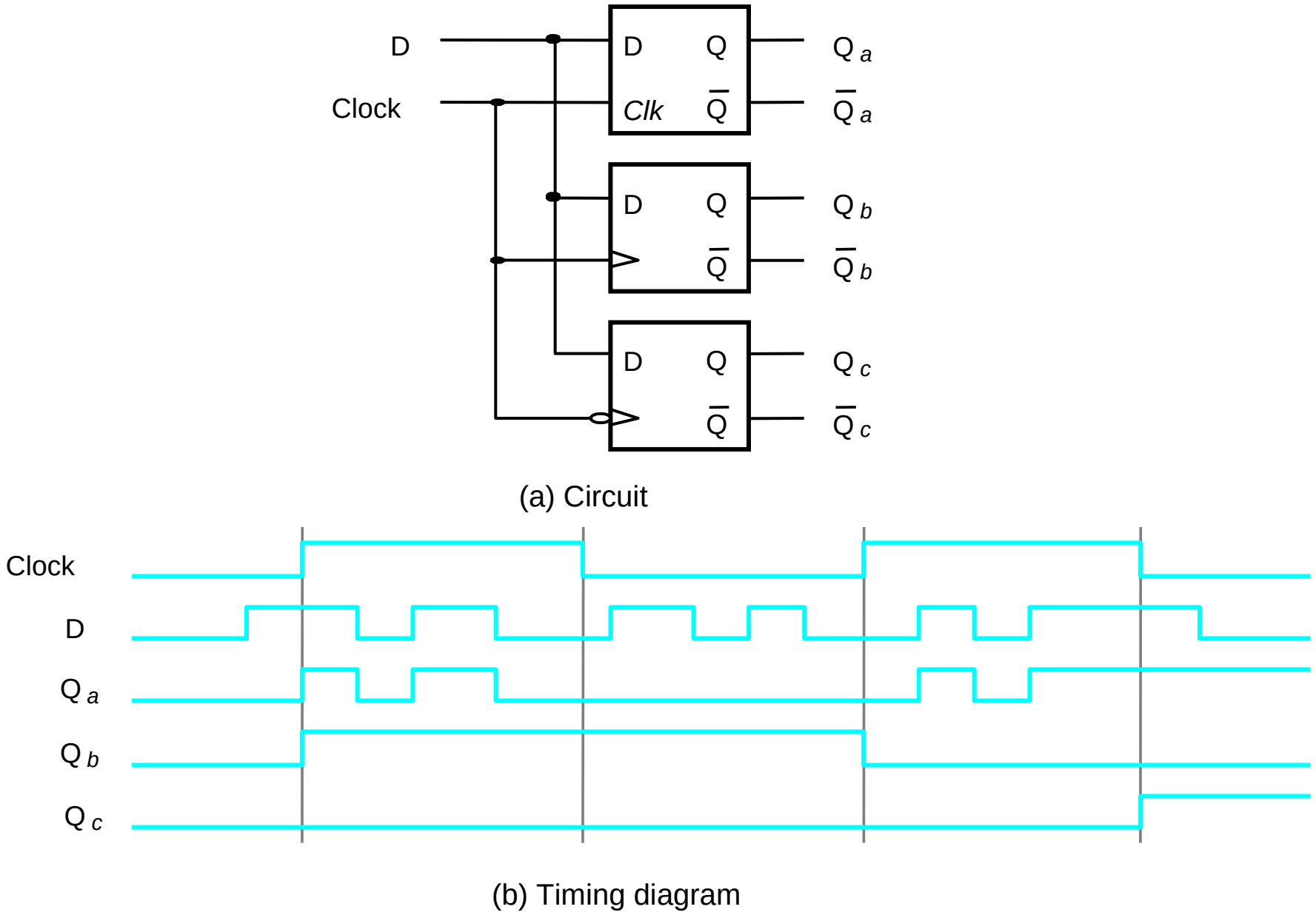


Figure 7.12. Comparison of level-sensitive and edge-triggered D storage elements.

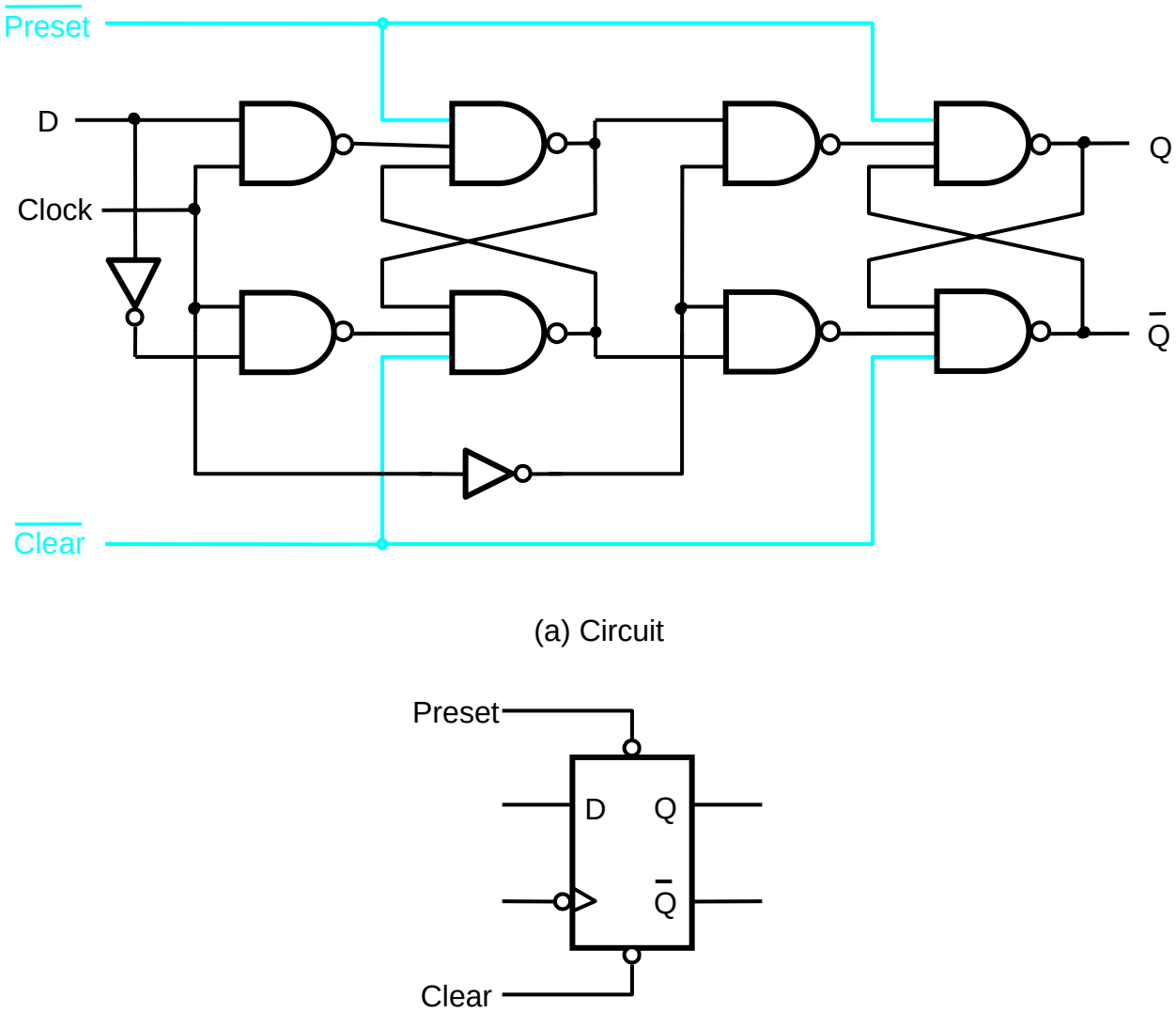
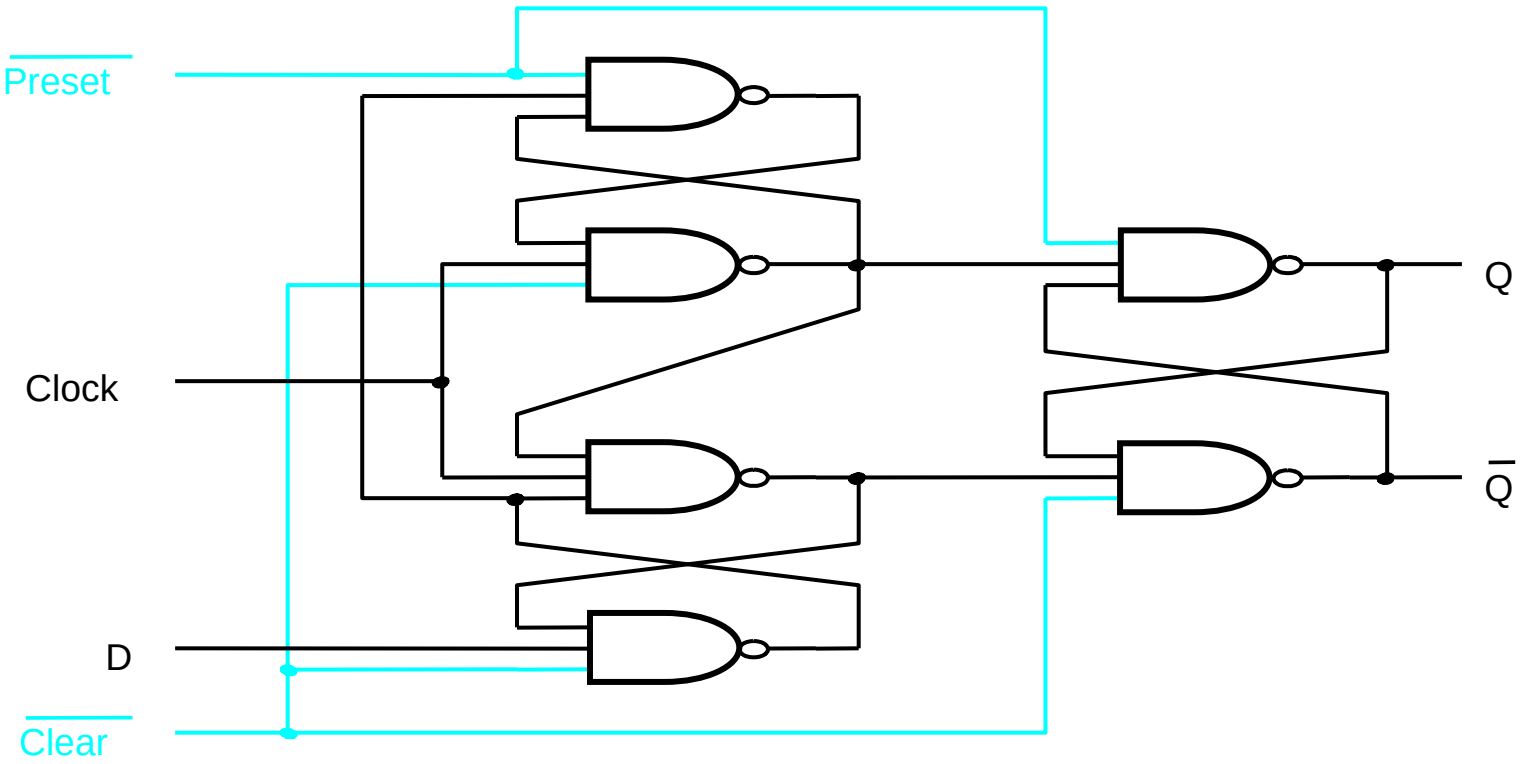
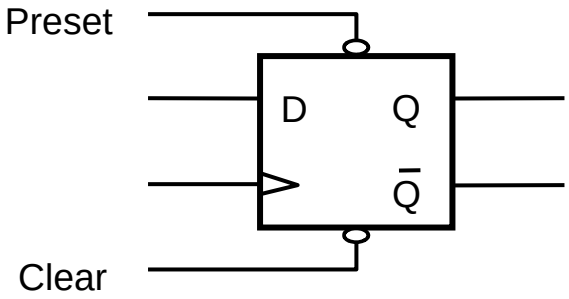


Figure 7.13. Master-slave D flip-flop with *Clear* and *Preset*.



(a) Circuit



(b) Graphical symbol

Figure 7.14. Positive-edge-triggered D flip-flop with *Clear* and *Preset*.

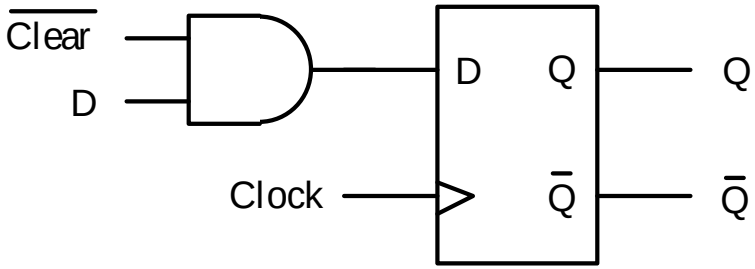
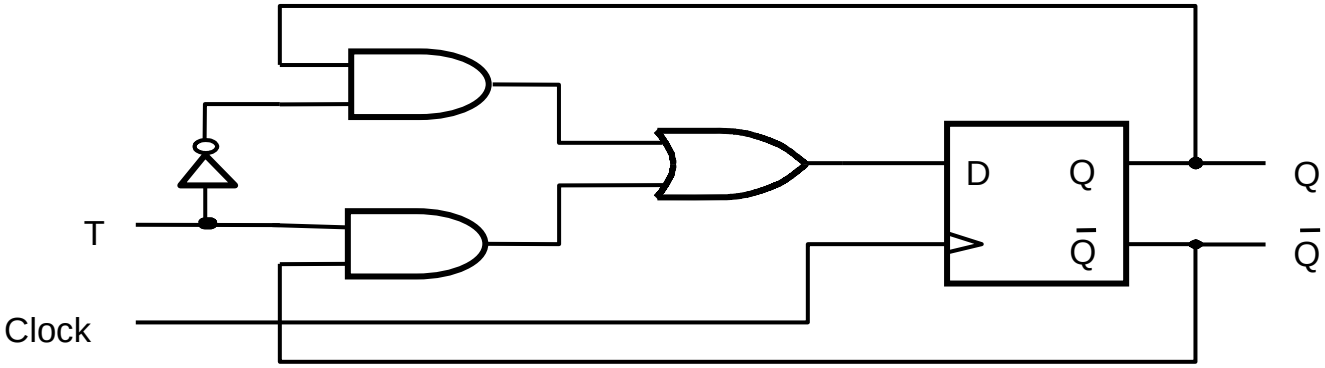


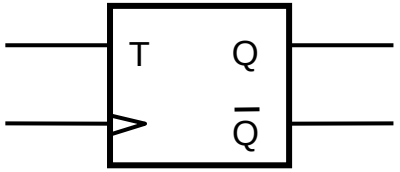
Figure 7.15. Synchronous reset for a D flip-flop.



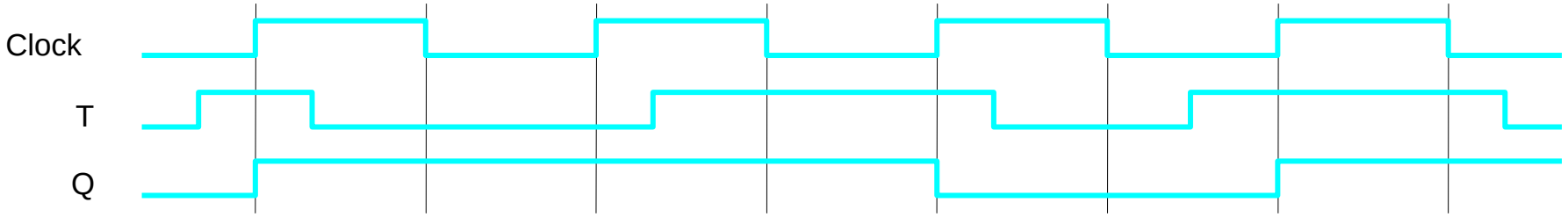
(a) Circuit

T	Q(t + 1)
0	Q(t)
1	Q(t)

(b) Truth table

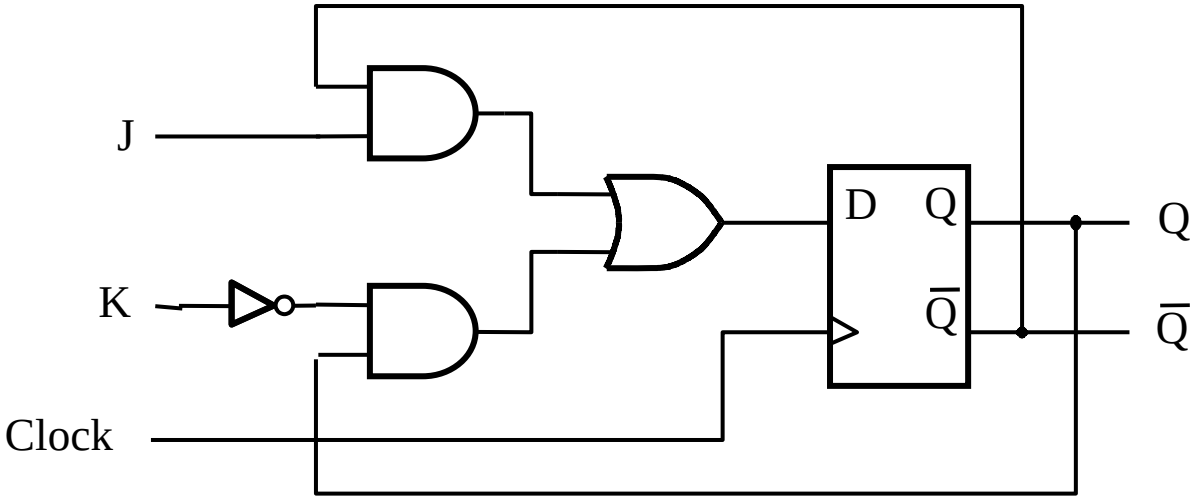


(c) Graphical symbol



(d) Timing diagram

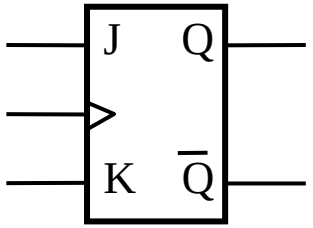
Figure 7.16. T flip-flop.



(a) Circuit

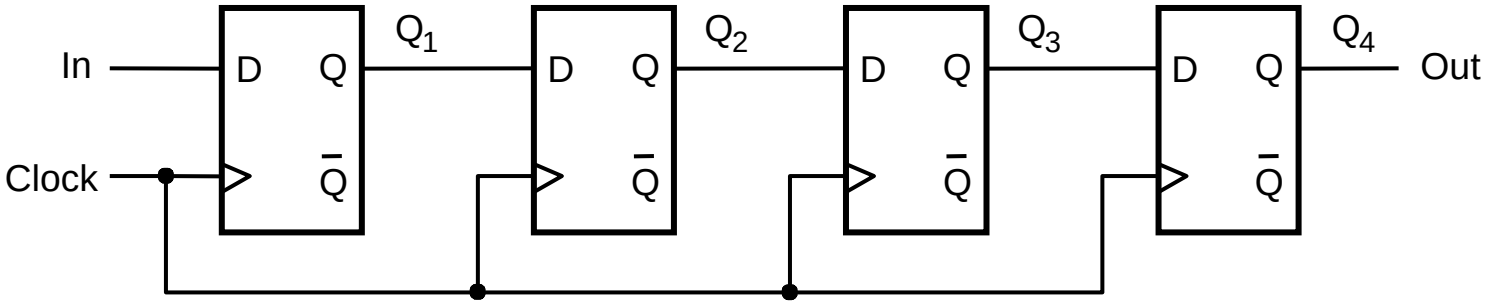
J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}(t)$

(b) Truth table



(c) Graphical symbol

Figure 7.17. JK flip-flop.



(a) Circuit

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

(b) A sample sequence

Figure 7.18. A simple shift register.

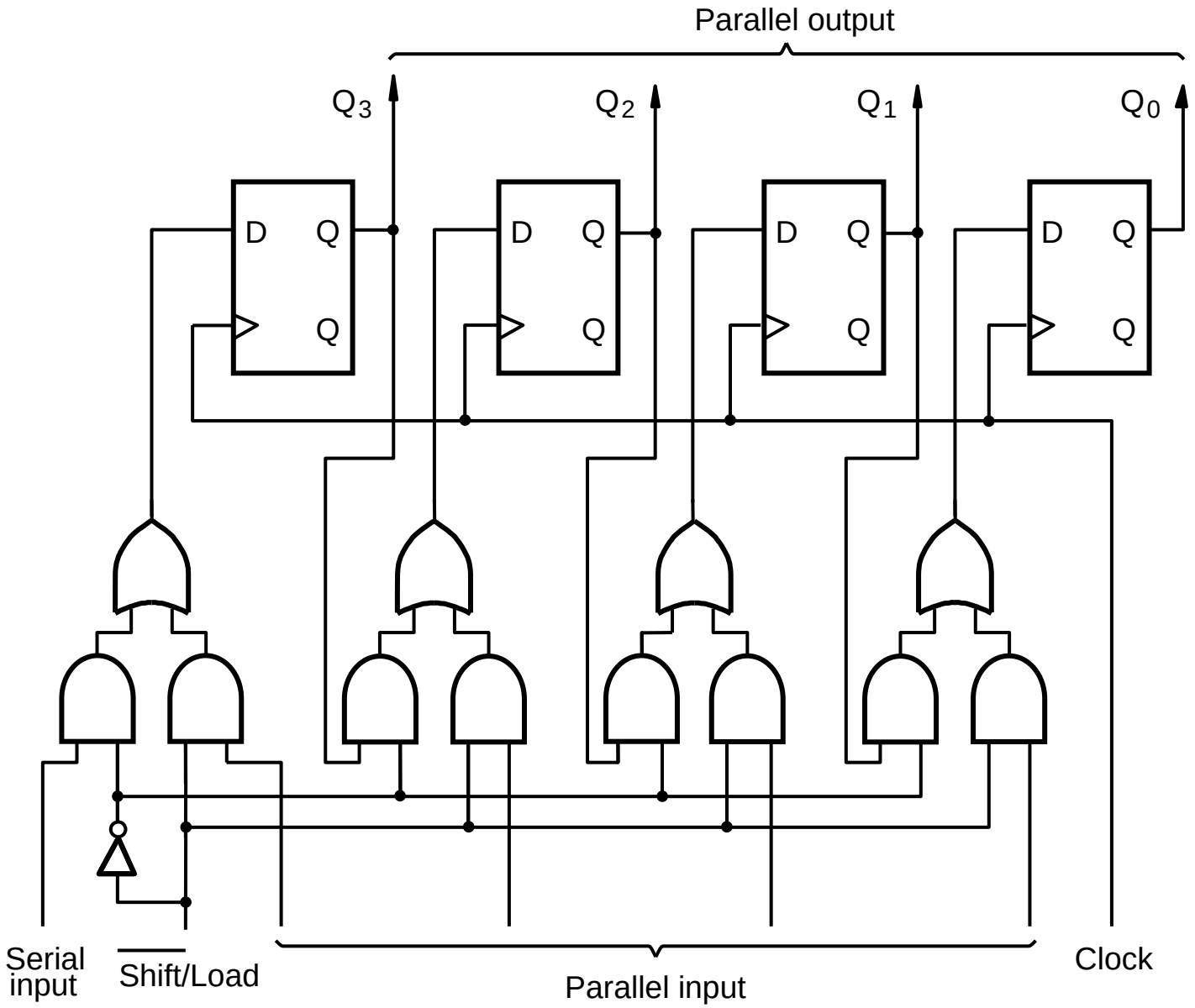


Figure 7.19. Parallel-access shift register.