SCE 0110 - Elementos de Lógica Digital I

Representação Numérica e Circuitos Aritméticos

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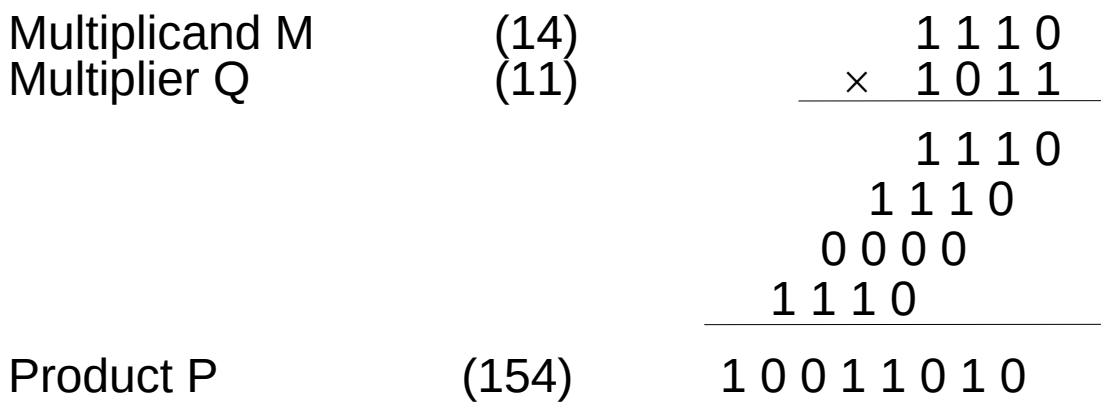
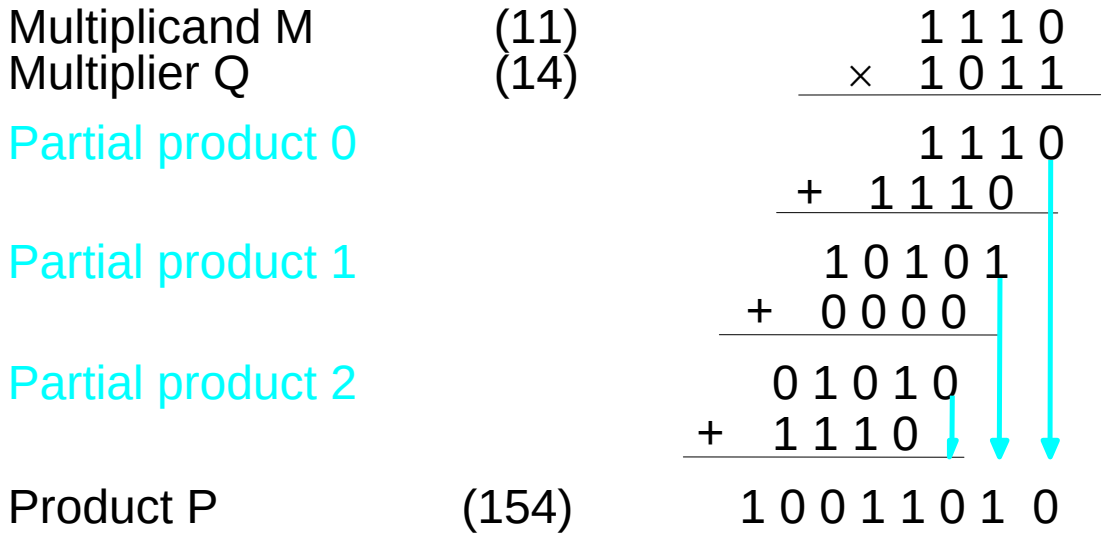


(a) Multiplication by hand

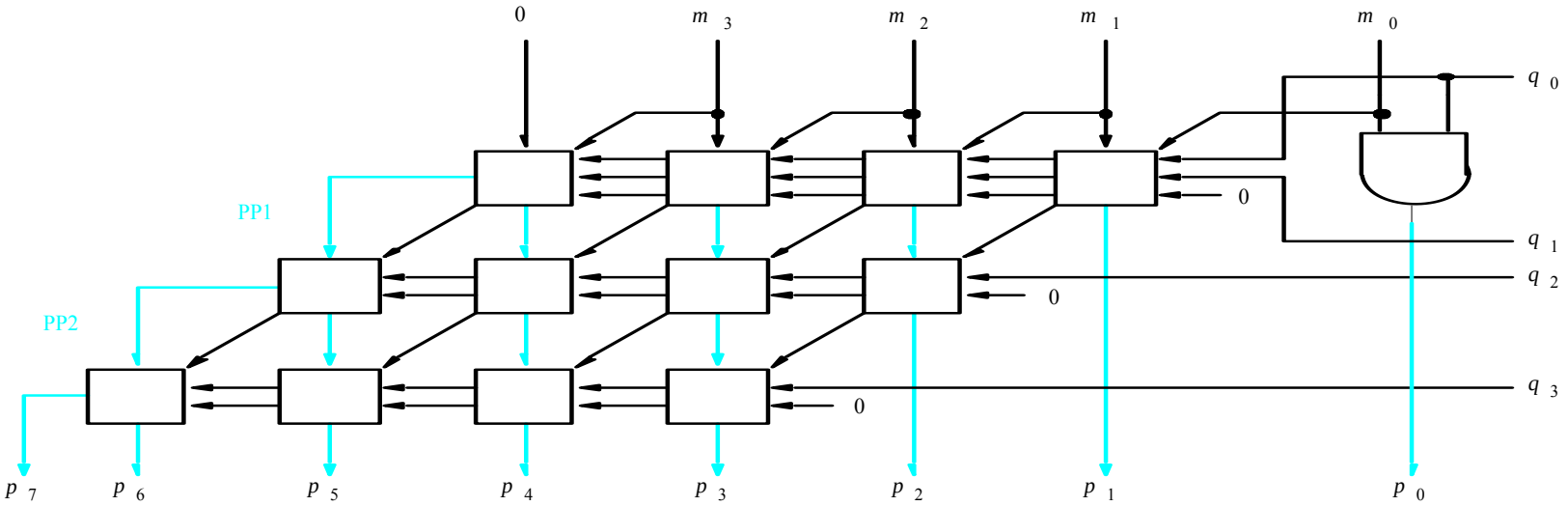
"uma abordagem sequencial simples precisaria de um somador de 8 bits"



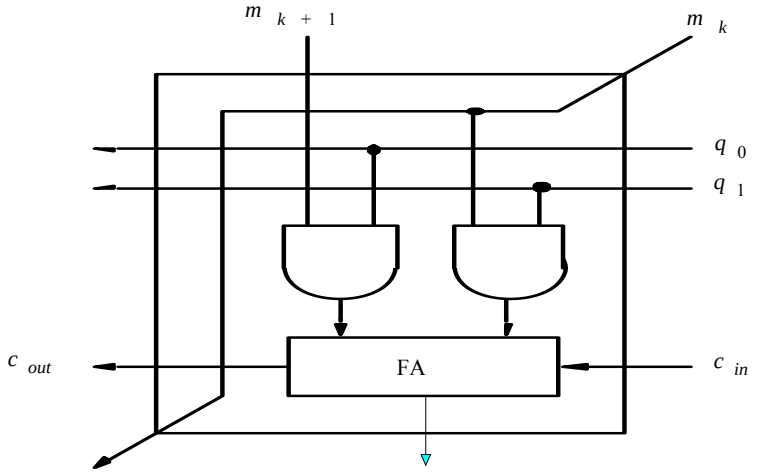
(b) Multiplication for implementation in hardware

"multiplicação utilizando vários somadores, nesse caso somadores de 4bits"

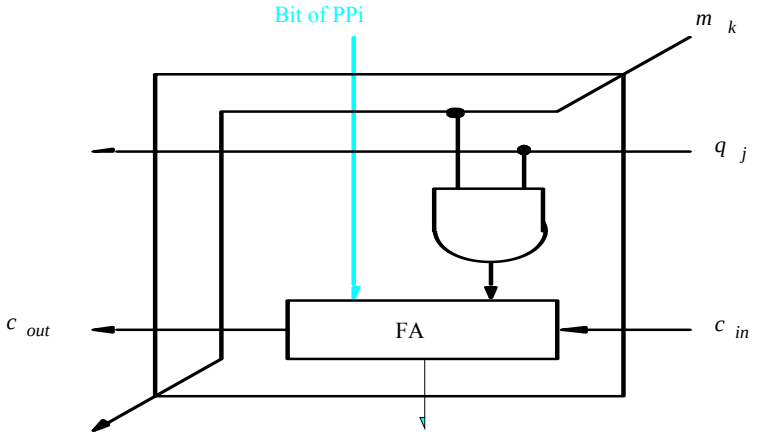
Figure 5.31. Multiplication of unsigned numbers.



(a) Structure of the circuit

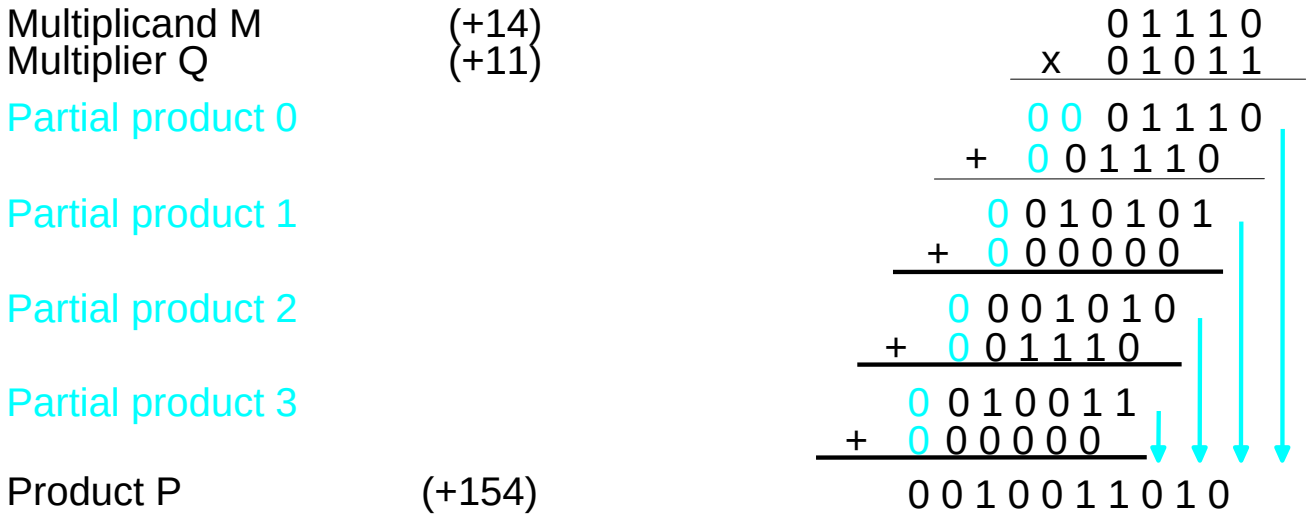


(b) A block in the top row

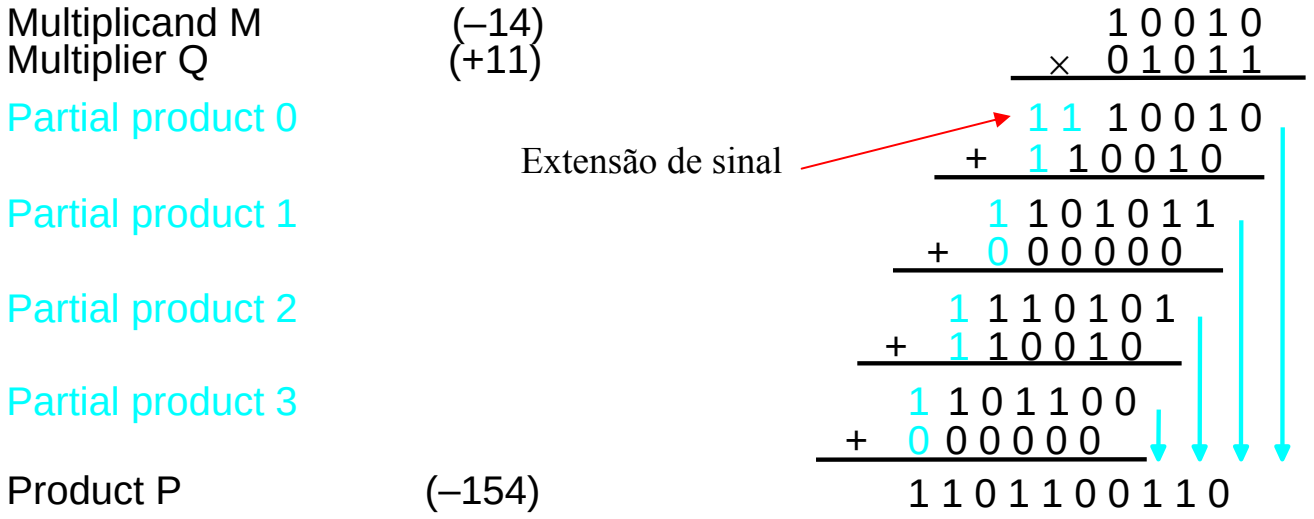


(c) A block in the bottom two rows

Figure 5.32. A 4 x 4 multiplier ciuciut.



(a) Positive multiplicand



(b) Negative multiplicand

Figure 5.33. Multiplication of signed numbers.

Fixed-Point Numbers

- Consist of an integer and fraction parts
- Can be written in the positional number representation

$$B = b_{n-1}b_{n-2}...b_1b_0.b_{-1}b_{-2}...b_{-k}$$

The value of the number is:

$$V(B) = \sum_{i=-k}^{n-1} b_i \times 2^i$$

- The radix point is considered to be fixed
- Logic circuits that deal with fixed-point are essentially the same as those used for integers

Floating-Point Numbers

- Aplicações científicas
  - Representação de números muito pequenos ou muito grandes
- Mantissa x $R^{Exponent}$
- Normalização
  - Ex.: 5.234×10^{43} ou 6.31×10^{-28}
- Padrão para números binários - IEEE754

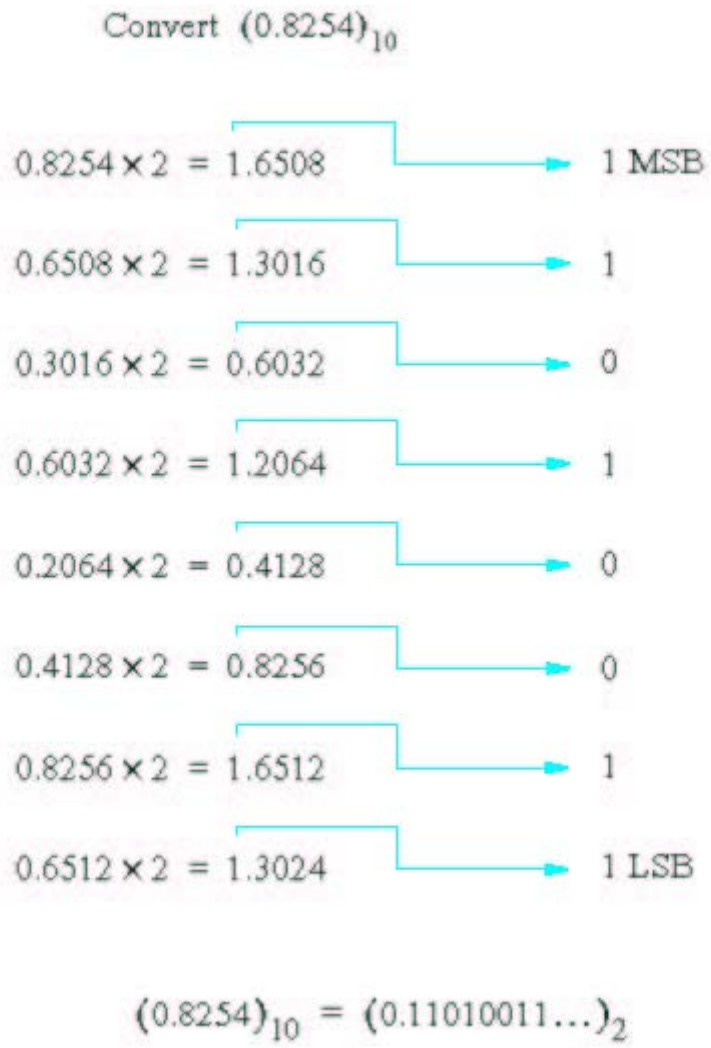


Figure 5.41. Conversion of fractions from decimal to binary.

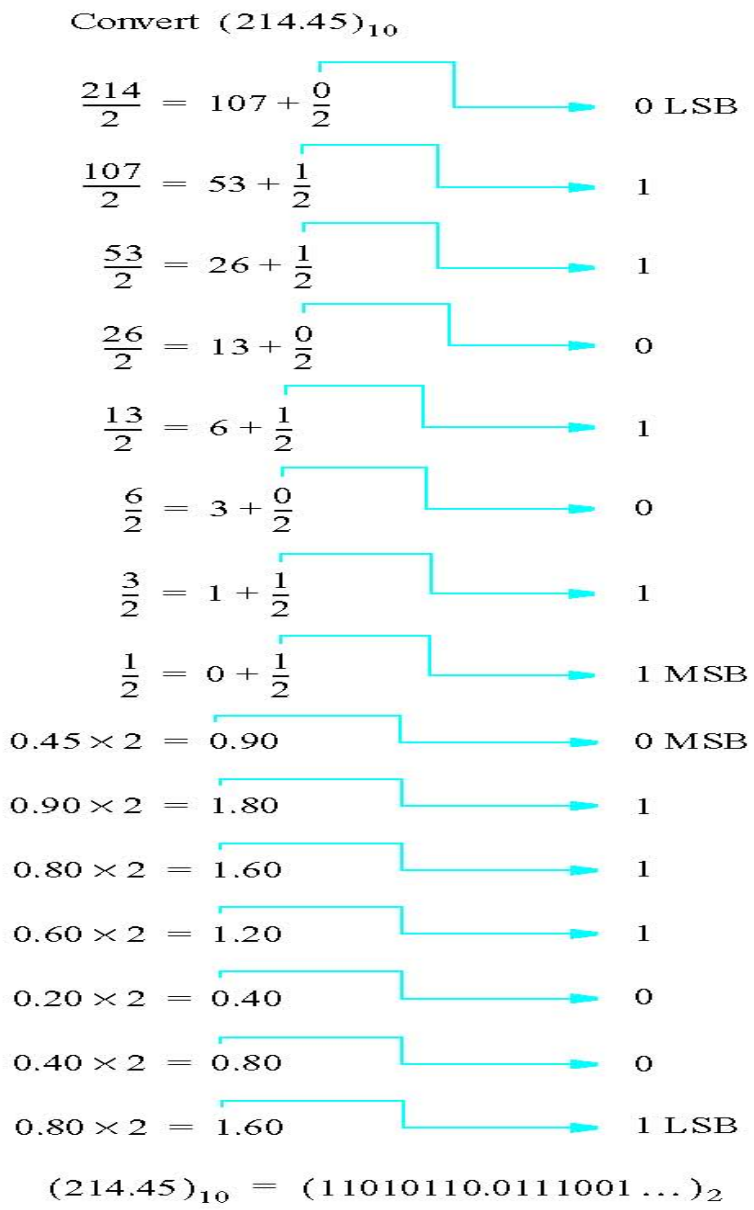


Figure 5.42. Conversion of fixed point numbers from decimal to binary.

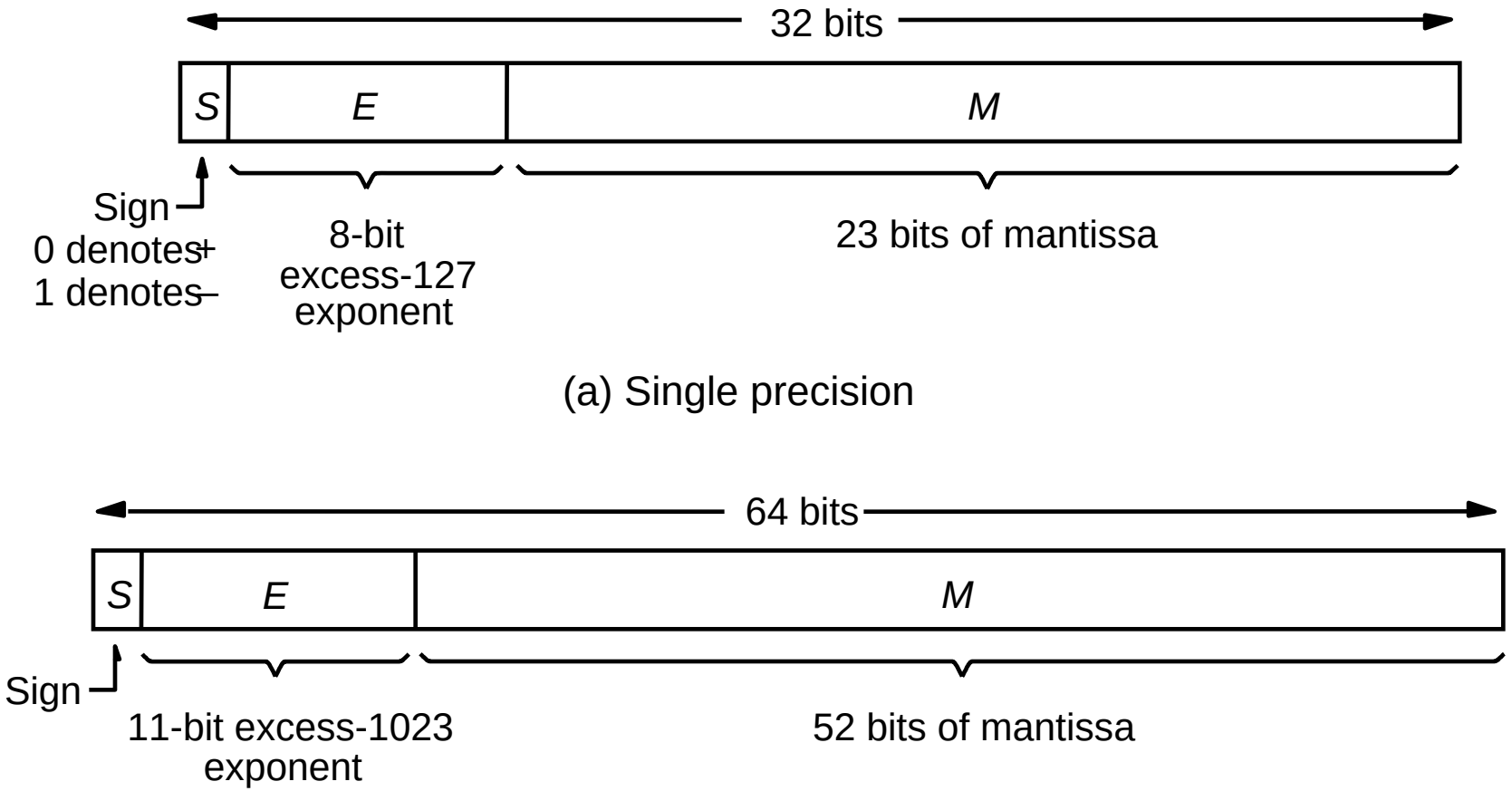
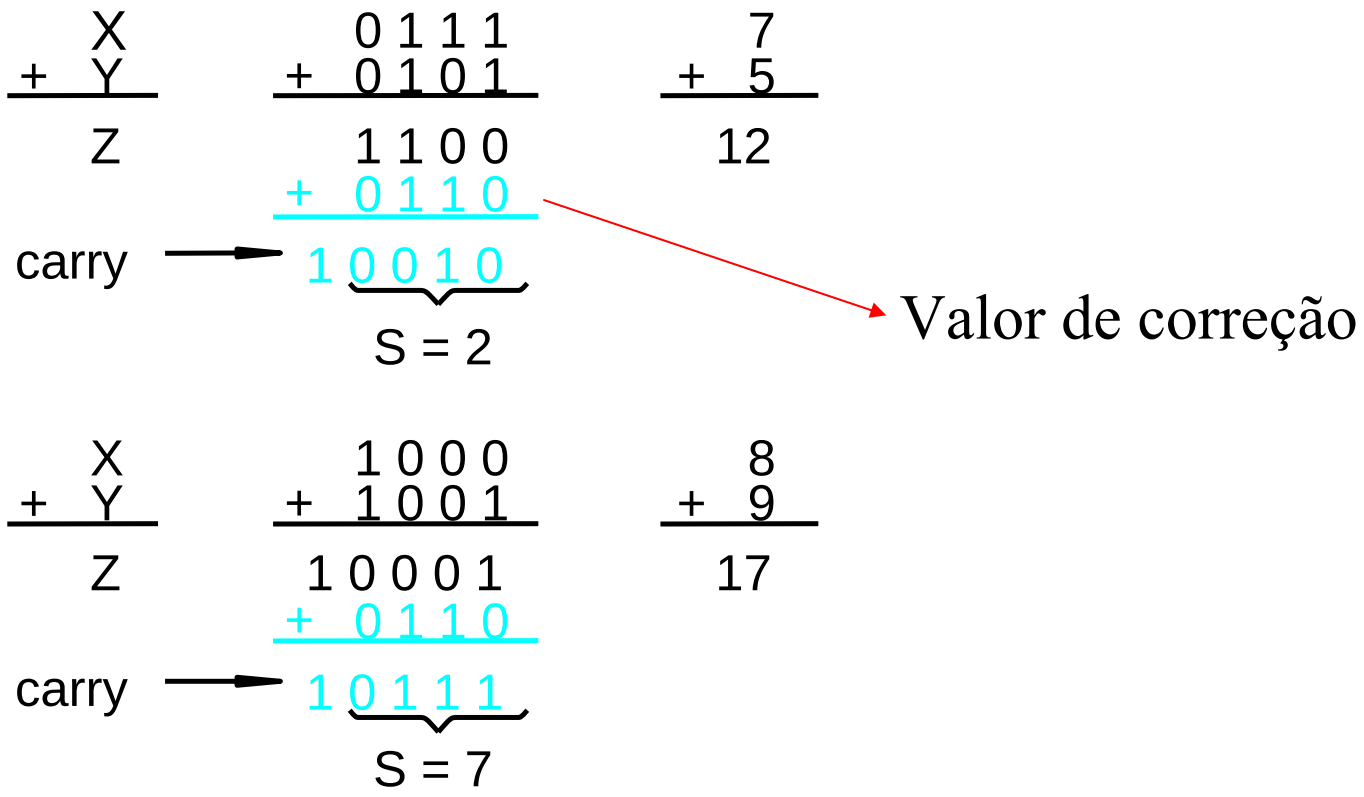


Figure 5.34. IEEE Standard floating-point formats.

Decimal digit	BCD code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

-Sobram 6 padrões
(desperdício de hardware)
-Circuitos aritméticos
-mais complexos

Table 5.3. Binary-coded decimal digits.



Como somar 10 + 10 em BCD?

Figure 5.35. Addition of BCD digits.

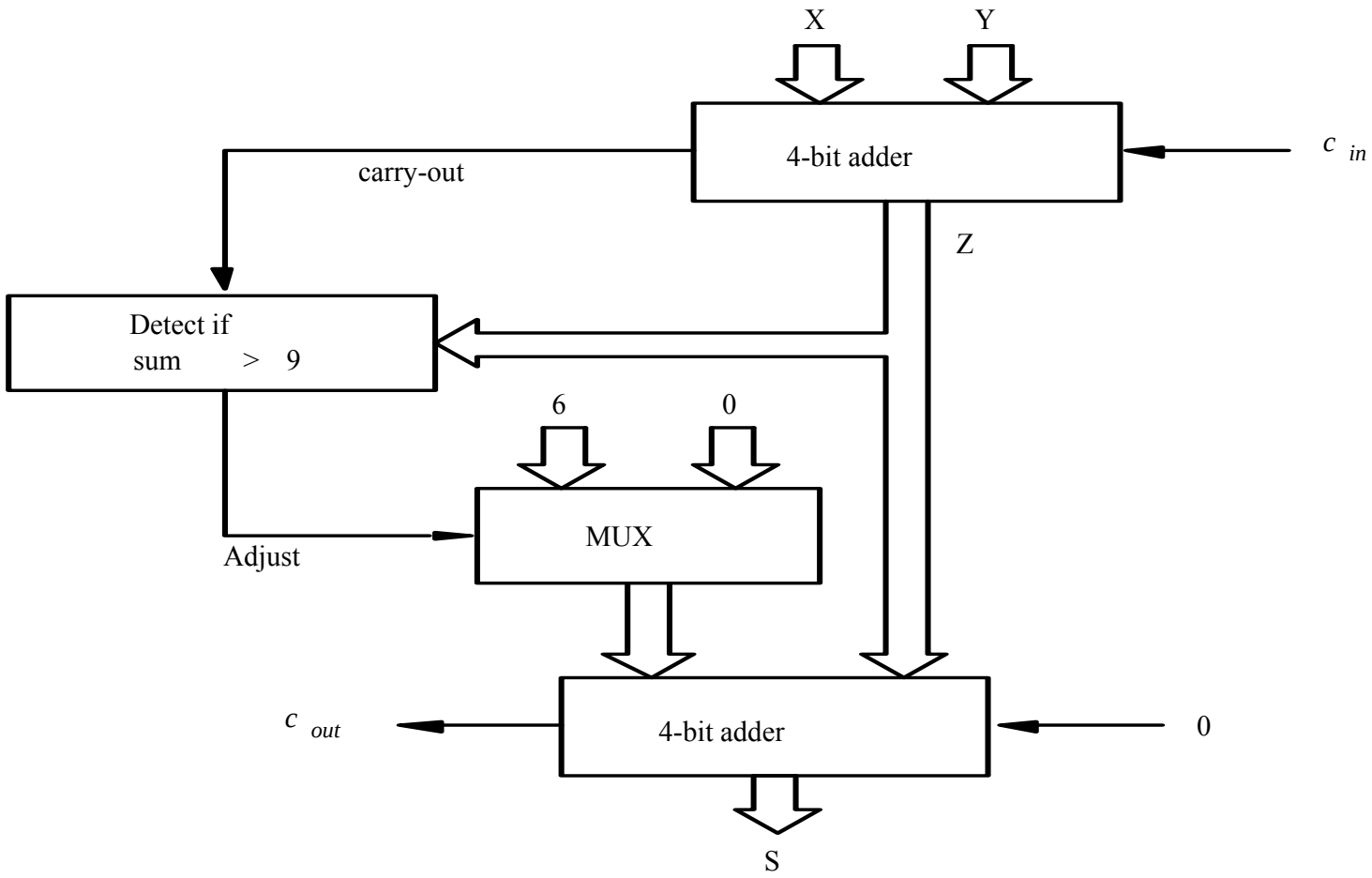


Figure 5.36. Block diagram for a one-digit BCD adder.

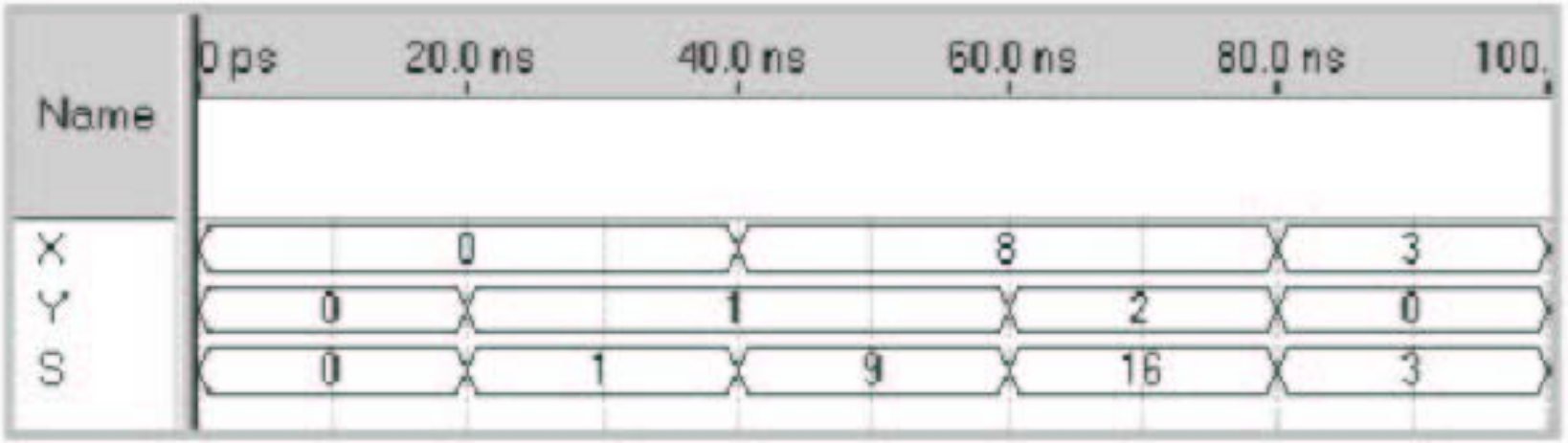


Figure 5.38. Functional simulation of the VHDL code in Figure 5.37.

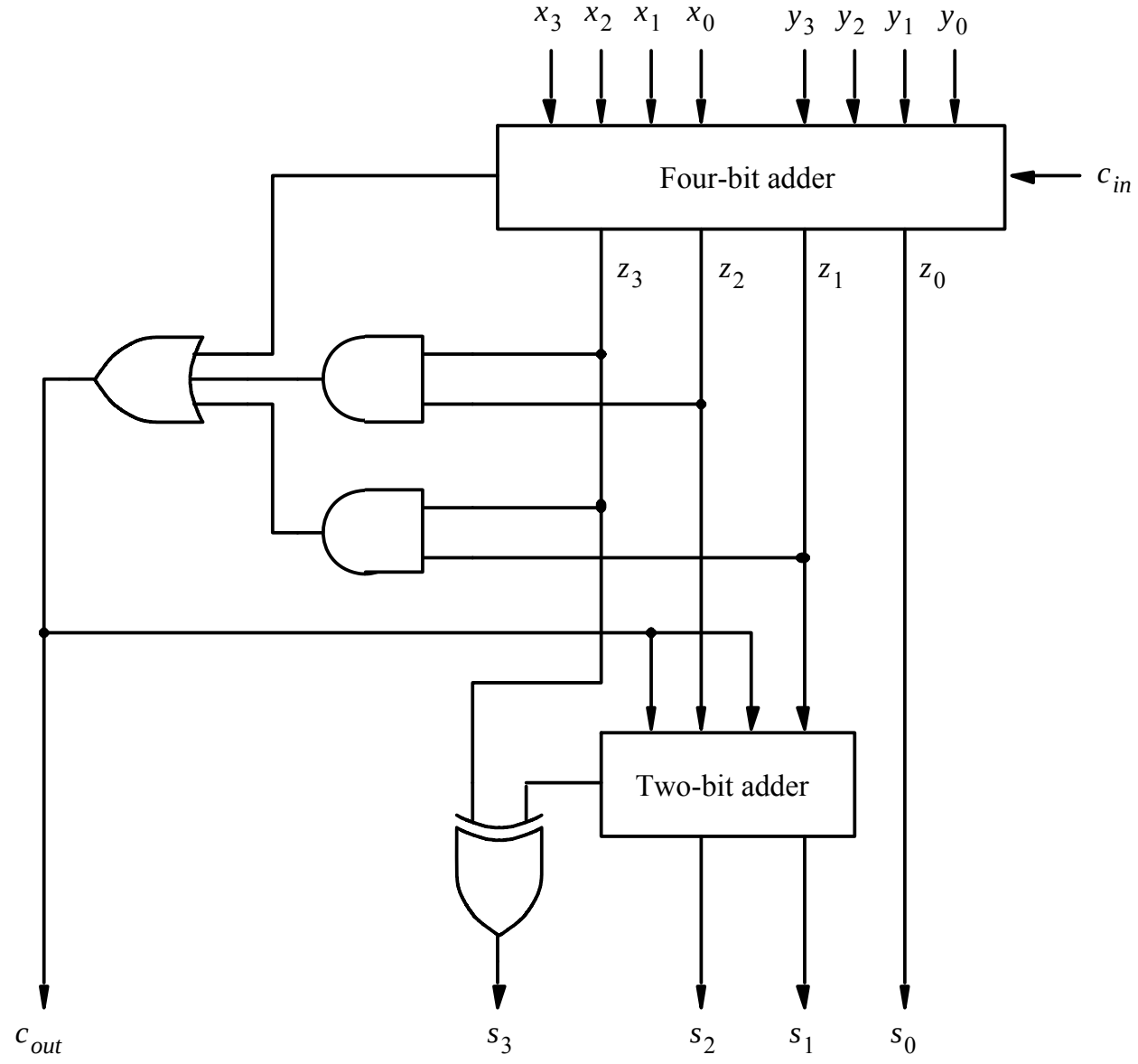


Figure 5.39. Circuit for a one-digit BCD adder.

Código ASCII

- Usado para codificar informações que são utilizadas como texto
- Não é conveniente para representar números que serão utilizados em operações aritméticas (melhor convertê-los para binário)
- Caracteres alfanuméricos (números e letras do alfabeto), pontuação e caracteres de controle
- ASCII utiliza 7 bits, podendo o bit 8 ser utilizado como bit de paridade

Tabela ASCII

Bit positions	Bit positions 654							
3210	000	001	010	011	100	101	110	111
0000	NUL	DLE	SPACE	0	@	P	´	p
0001	SOH	DC1	!	1	A	Q	a	q
0010	STX	DC2	”	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK	SYN	&	6	F	V	f	v
0111	BEL	ETB	’	7	G	W	g	w
1000	BS	CAN	(	8	H	X	h	x
1001	HT	EM	)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[	k	{
1100	FF	FS	,	<	L	\	1	|
1101	CR	GS	-	=	M	]	m	}
1110	SO	RS	.	>	N	^	n	~
1111	SI	US	/	?	O	—	o	DEL

NUL	Null/Idle	SI	Shift in
SOH	Start of header	DLE	Data link escape
STX	Start of text	DC1-DC4	Device control
ETX	End of text	NAK	Negative acknowledgement
EOT	End of transmission	SYN	Synchronous idle
ENQ	Enquiry	ETB	End of transmitted block
ACQ	Acknowledgement	CAN	Cancel (error in data)
BEL	Audible signal	EM	End of medium
BS	Back space	SUB	Special sequence
HT	Horizontal tab	ESC	Escape
LF	Line feed	FS	File separator
VT	Vertical tab	GS	Group separator
FF	Form feed	RS	Record separator
CR	Carriage return	US	Unit separator
SO	Shift out	DEL	Delete/Idle

Bit positions of code format = | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Table 5.4. The seven-bit ASCII code (7 bits).

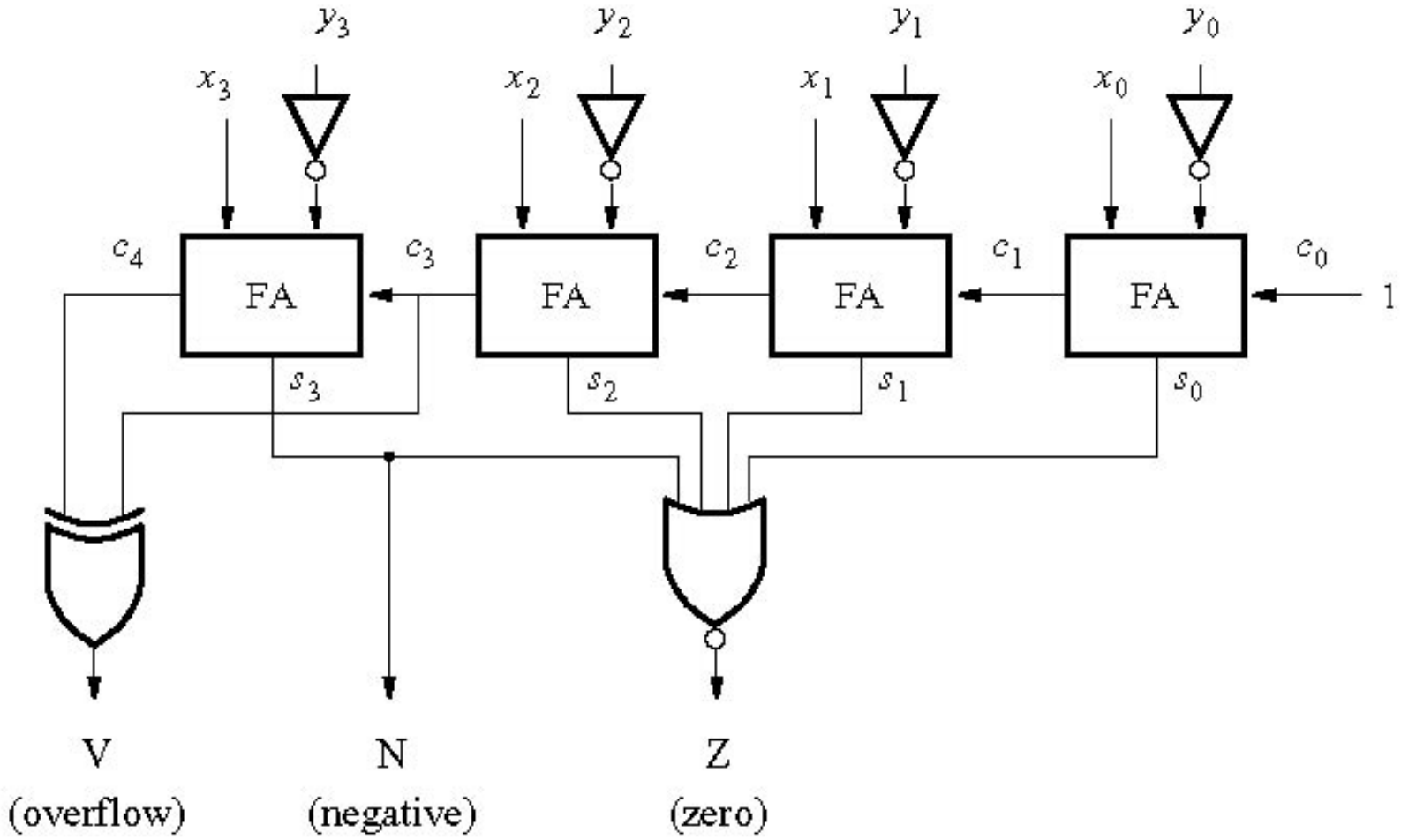


Figure 5.43. A comparator circuit.