

# SCE 0110 - Elementos de Lógica Digital I

**Blocos de construção  
de circuitos combinacionais  
(continuação)**

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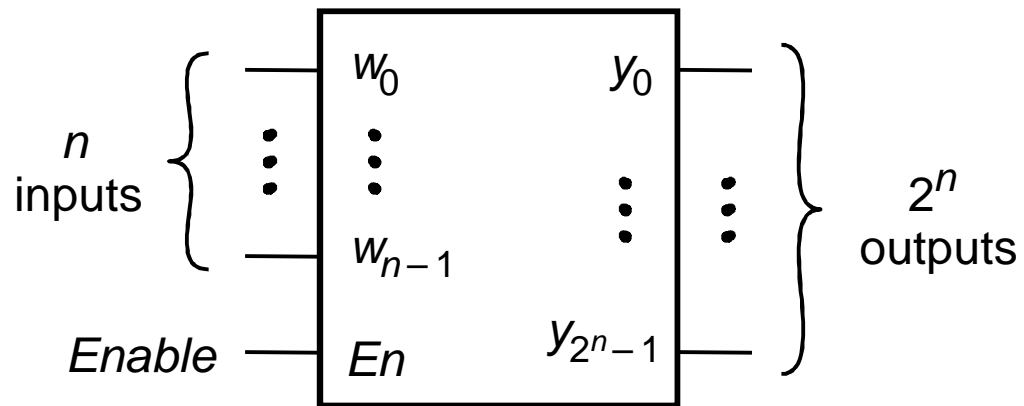
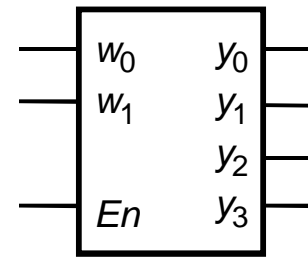


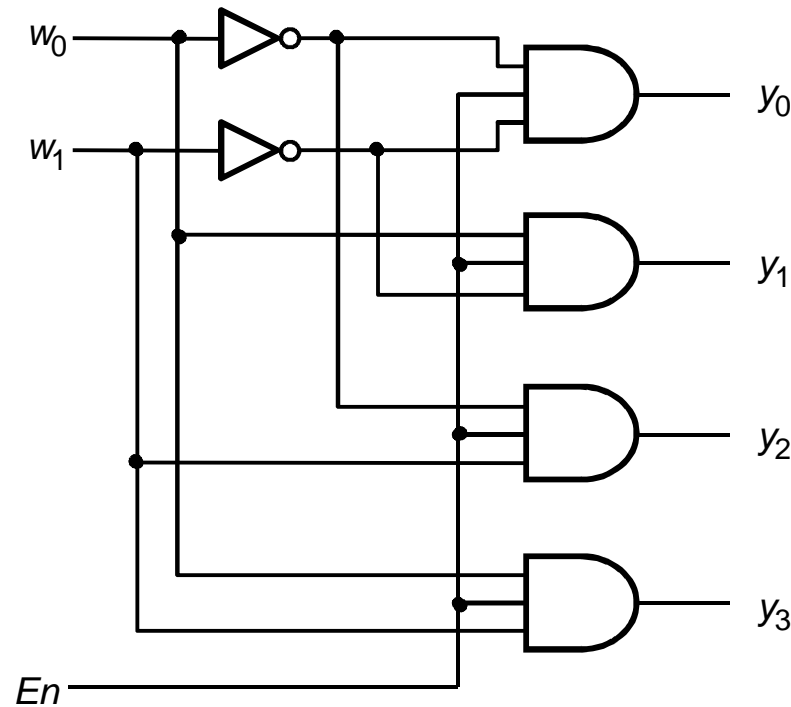
Figure 6.15. An  $n$ -to- $2^n$  binary decoder.

$En$	$w_1$	$w_0$	$y_0$	$y_1$	$y_2$	$y_3$
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a) Truth table



(b) Graphical symbol



(c) Logic circuit

Figure 6.16. A 2-to-4 decoder.

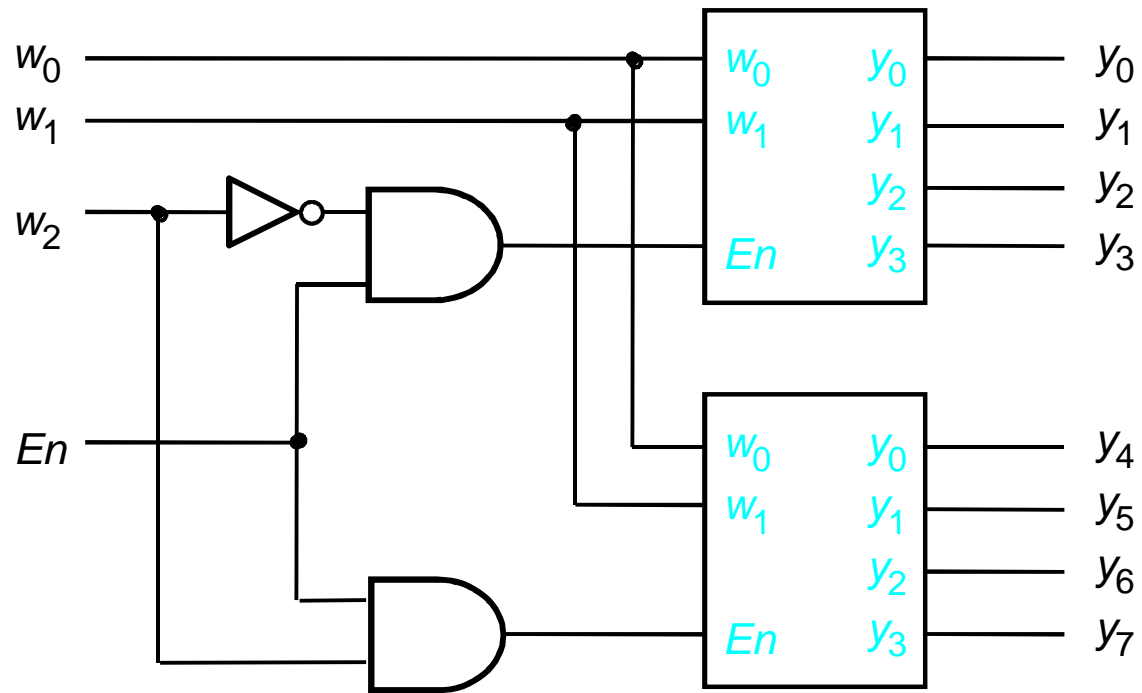


Figure 6.17. A 3-to-8 decoder using two 2-to-4 decoders.

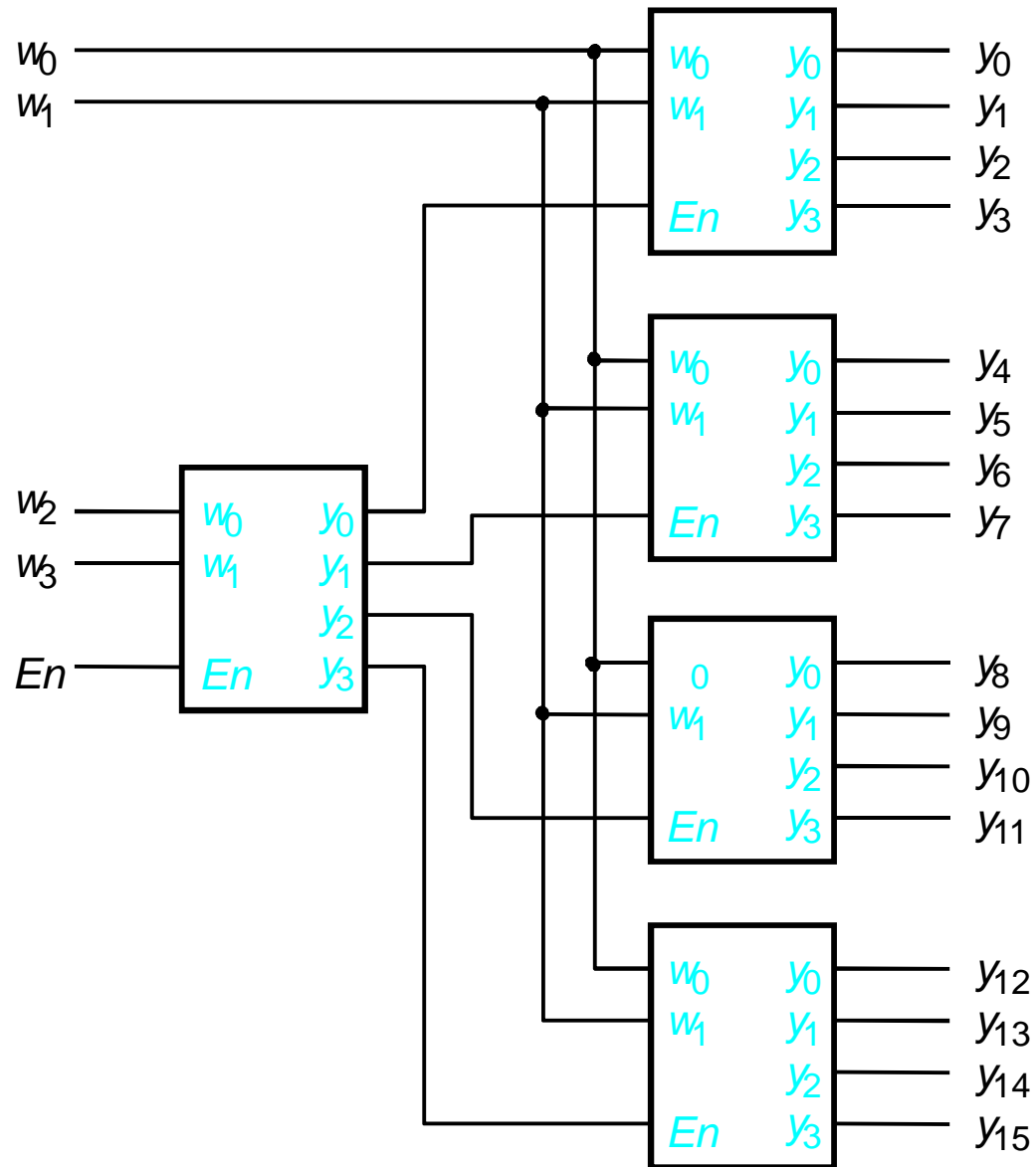


Figure 6.18. A 4-to-16 decoder built using a decoder tree.

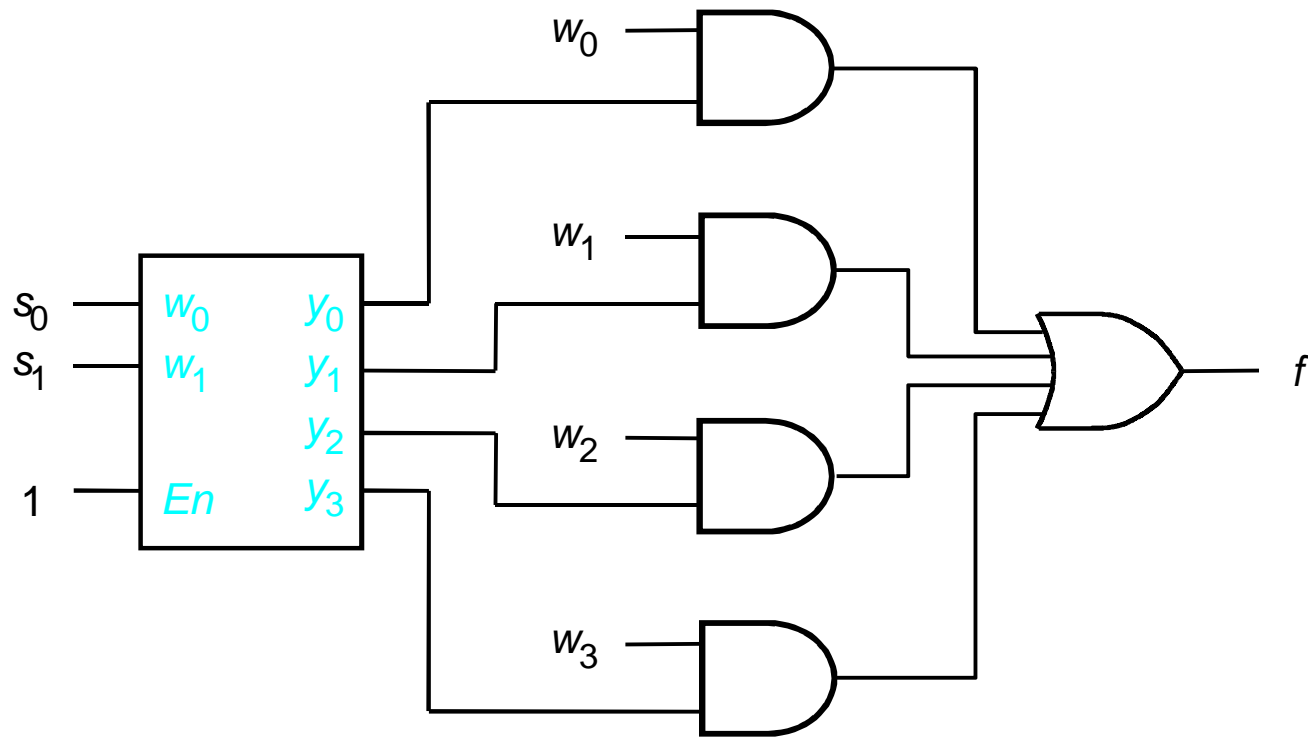


Figure 6.19. A 4-to-1 multiplexer built using a decoder.

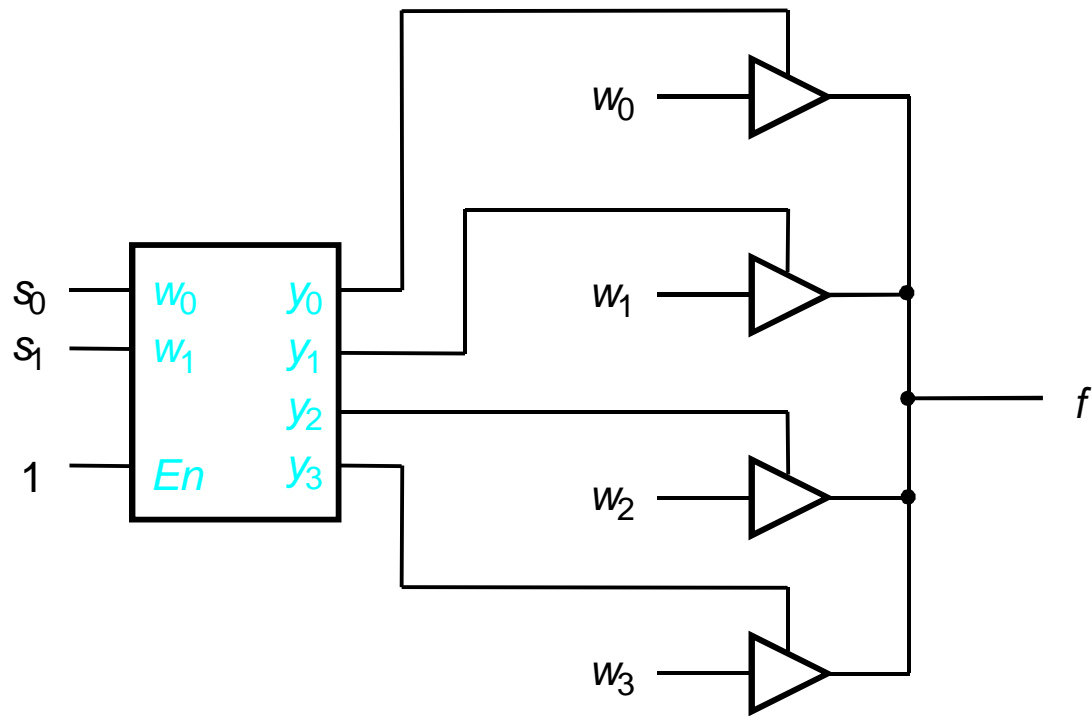


Figure 6.20. A 4-to-1 multiplexer built using a decoder and tri-state buffers.

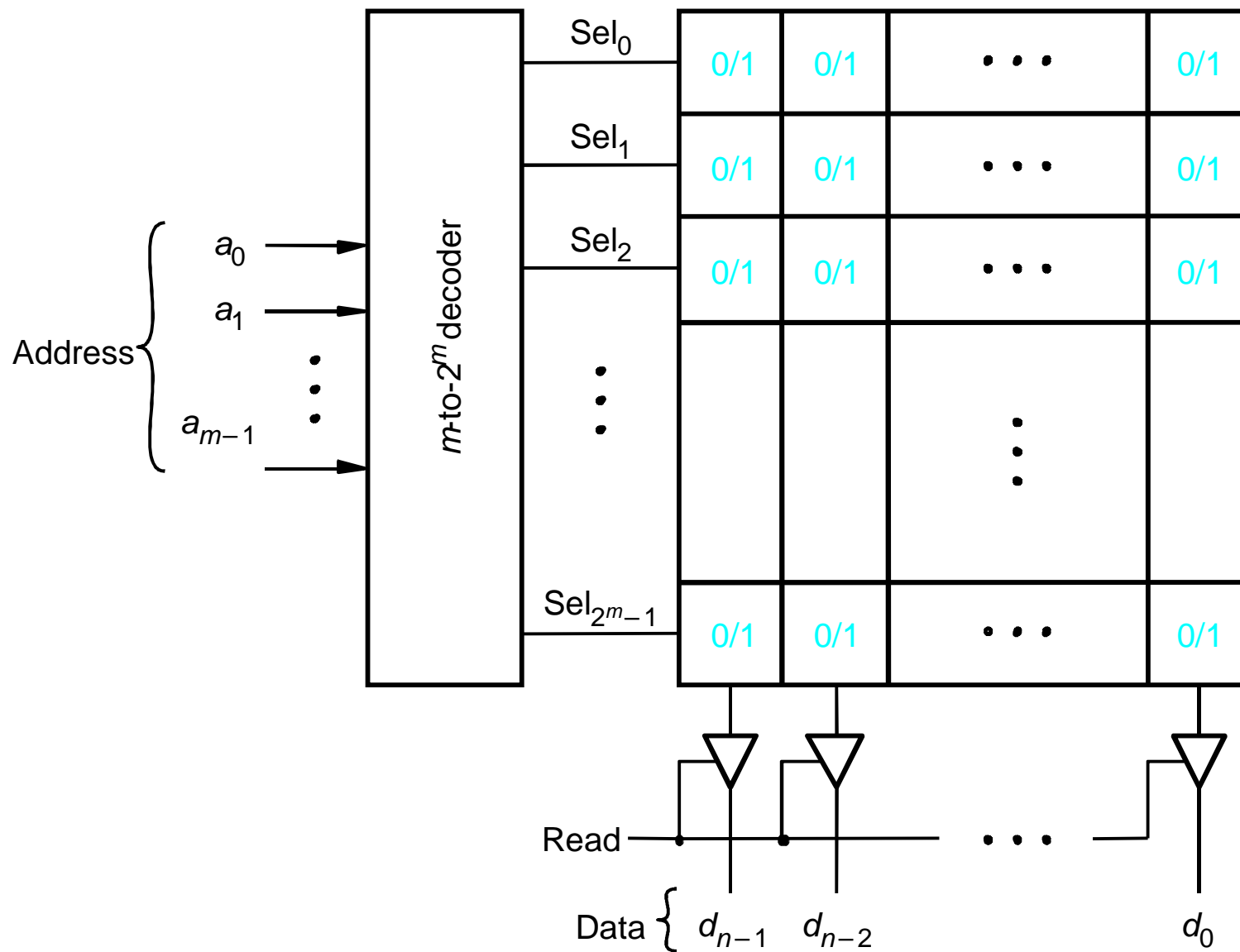


Figure 6.21. A  $2^m \times n$  read-only memory (ROM) block.



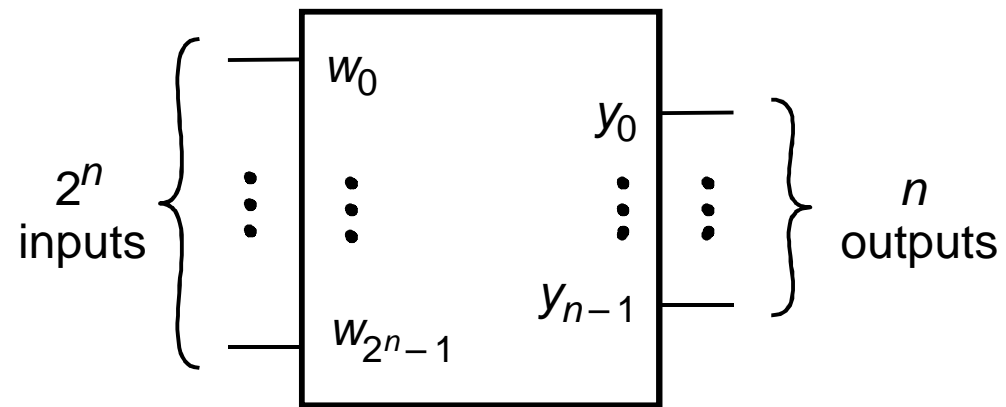
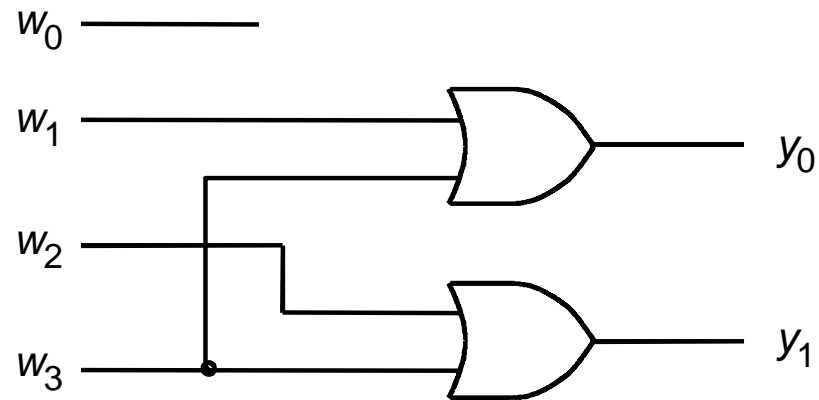


Figure 6.22. A  $2^n$ -to- $n$  binary encoder.

$w_3$	$w_2$	$w_1$	$w_0$	$y_1$	$y_0$
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

(a) Truth table

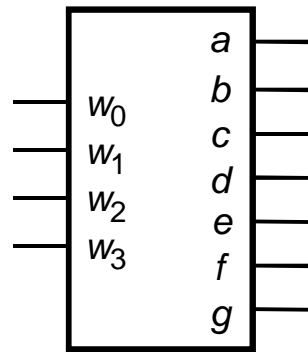


(b) Circuit

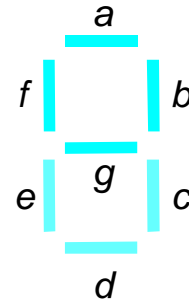
Figure 6.23. A 4-to-2 binary encoder.

$w_3$	$w_2$	$w_1$	$w_0$	$y_1$	$y_0$	$z$
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Figure 6.24. Truth table for a 4-to-2 priority encoder.



(a) Code converter



(b) 7-segment display

$w_3$	$w_2$	$w_1$	$w_0$	$a$	$b$	$c$	$d$	$e$	$f$	$g$
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

(c) Truth table

Figure 6.25. A BCD-to-7-segment display code converter.

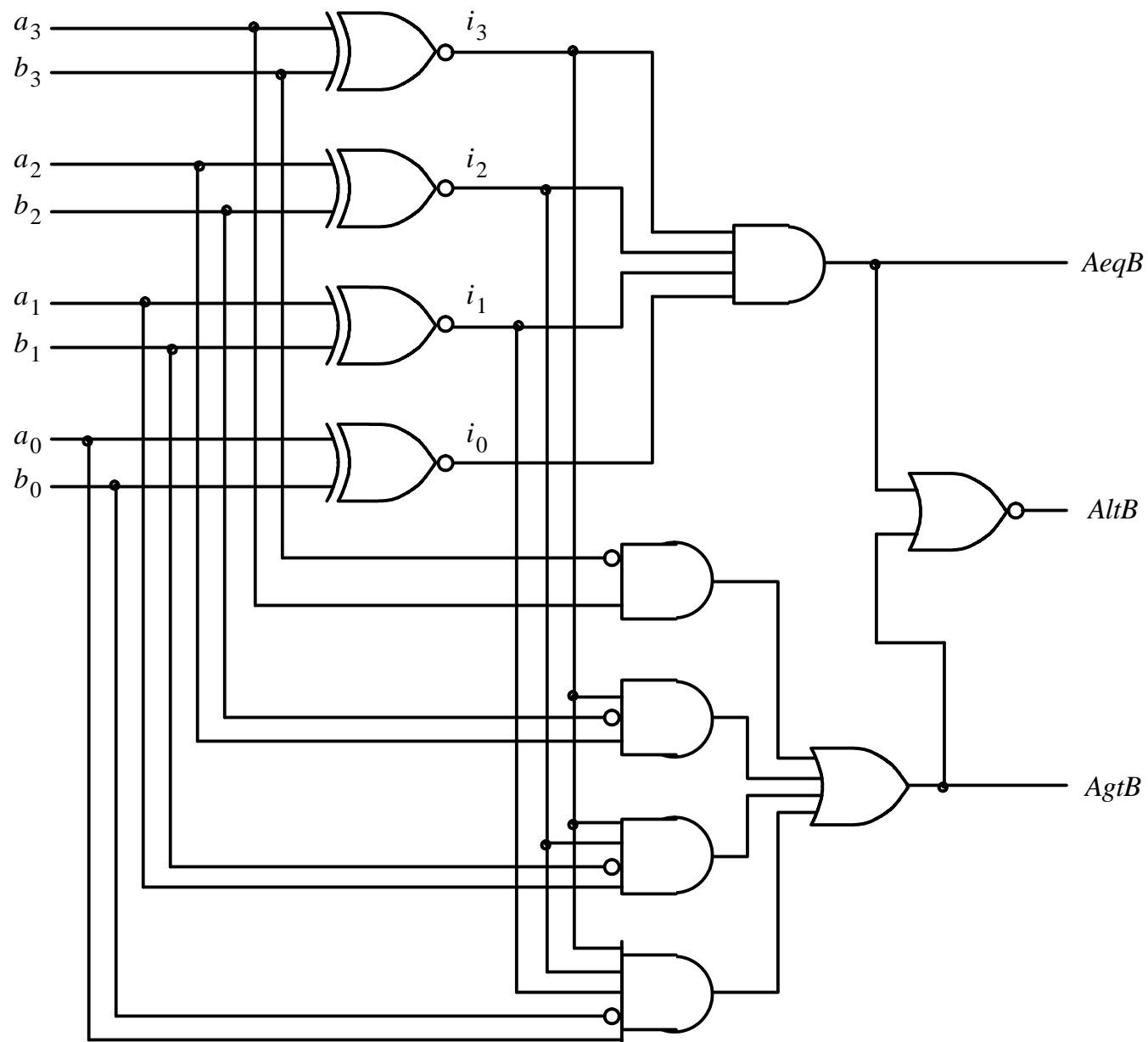


Figure 6.26. A four-bit comparator circuit.

# Exercícios

- Examples
  - 6.25, 6.26, 6.27, 6.28, 6.30, 6.31

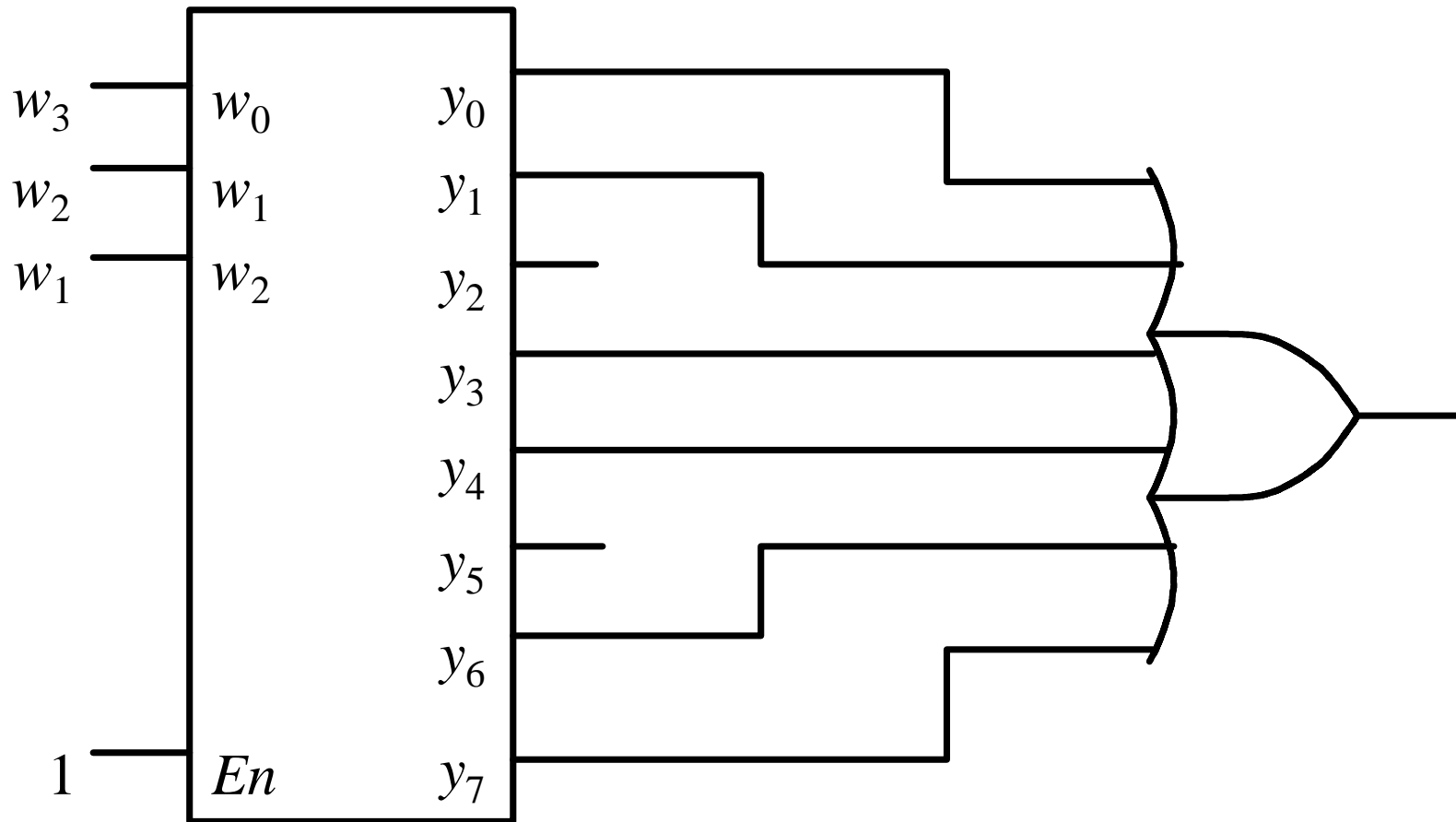


Figure 6.50. Circuit for Example 6.25.

$w_7$	$w_6$	$w_5$	$w_4$	$w_3$	$w_2$	$w_1$	$w_0$	$y_2$	$y_1$	$y_0$
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Figure 6.51. Truth table for an 8-to-3 binary encoder.



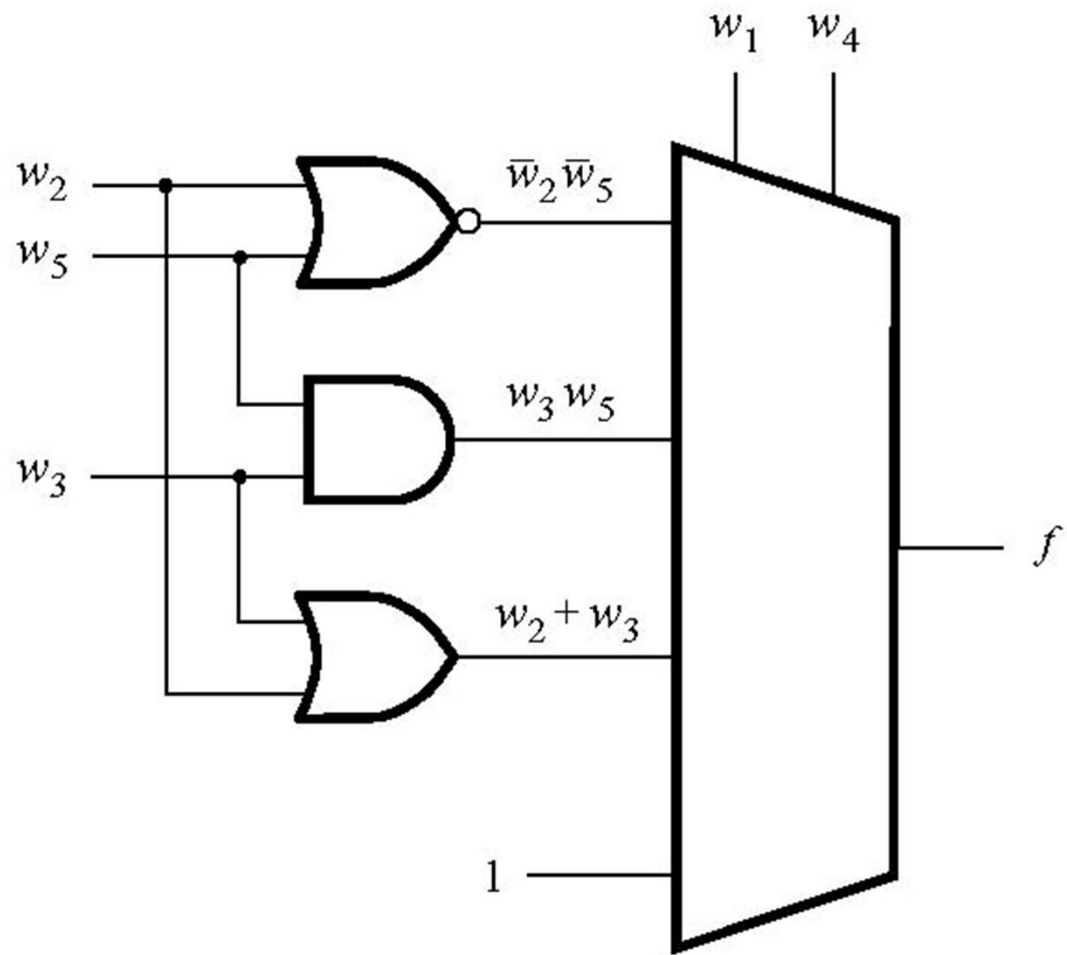
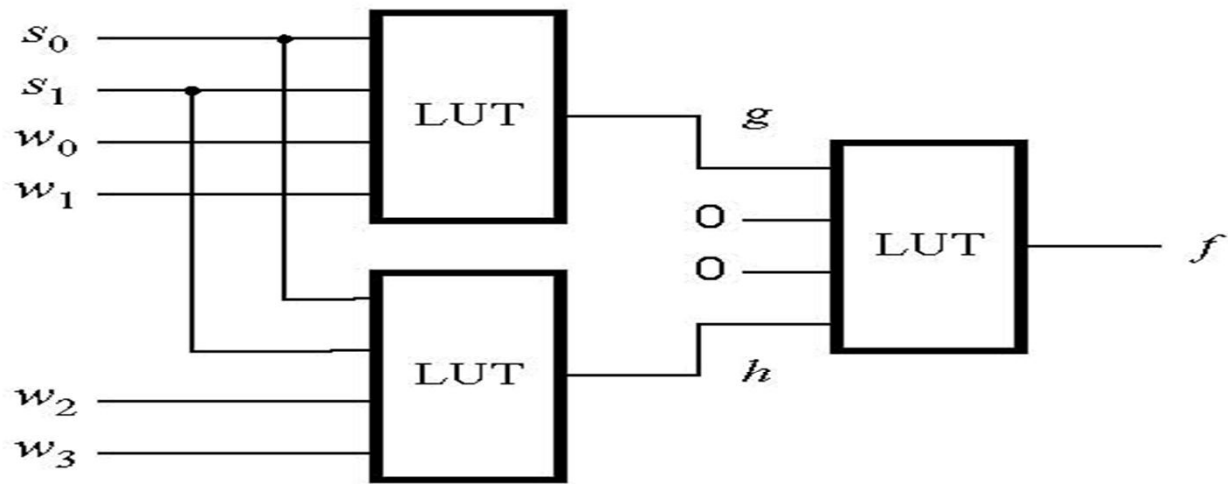


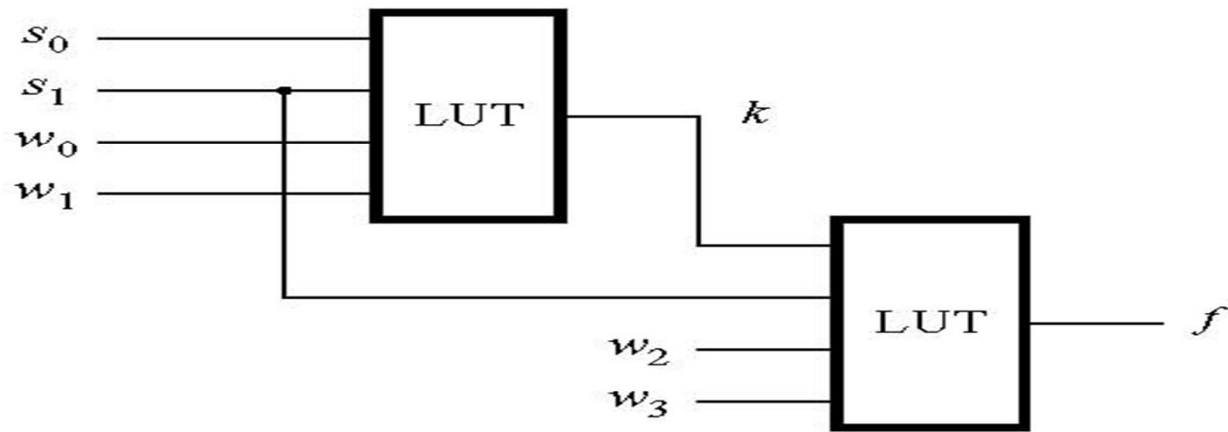
Figure 6.52. Circuit for Example 6.27.

$b_2$	$b_1$	$b_0$	$g_2$	$g_1$	$g_0$
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Figure 6.53. Binary to Gray code conversion.



(a) Using three LUTs



(b) Using two LUTs

Figure 6.55. Circuits for Example 6.30.

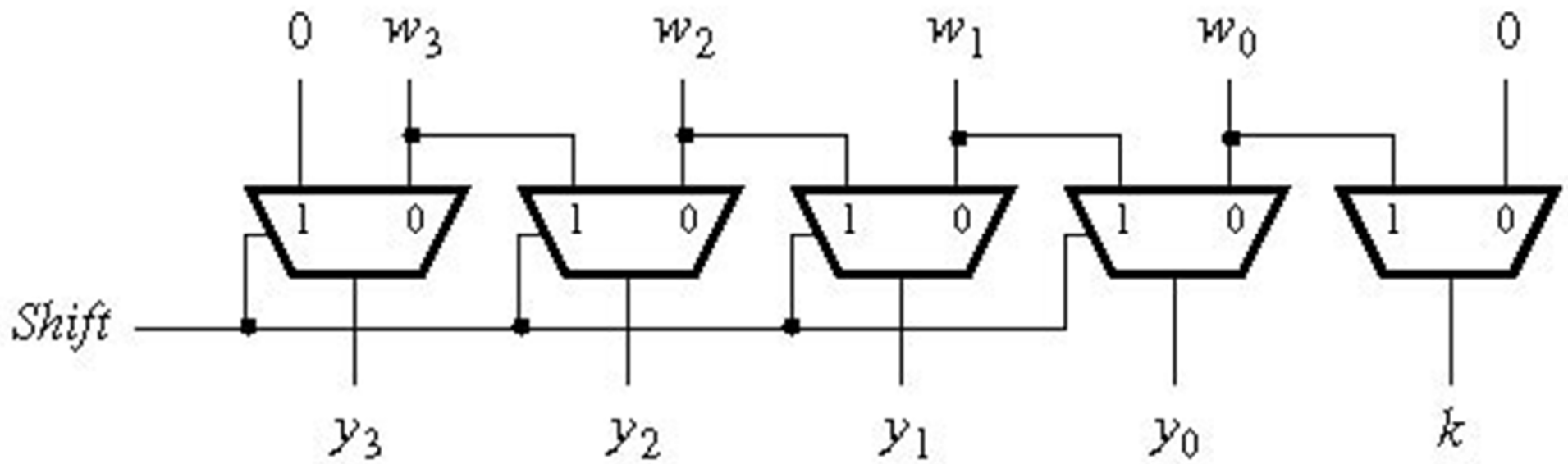
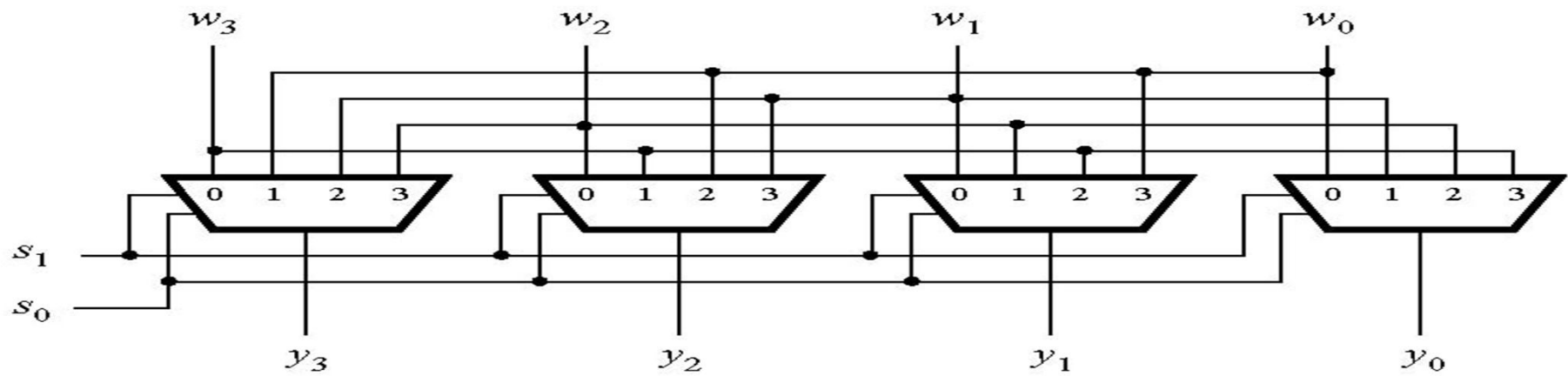


Figure 6.56. A shifter circuit.

$s_1$	$s_0$	$y_3$	$y_2$	$y_1$	$y_0$
0	0	$w_3$	$w_2$	$w_1$	$w_0$
0	1	$w_0$	$w_3$	$w_2$	$w_1$
1	0	$w_1$	$w_0$	$w_3$	$w_2$
1	1	$w_2$	$w_1$	$w_0$	$w_3$

(a) Truth table



(b) Circuit

Figure 6.57. A barrel shifter circuit.