

SCE 0117 - Introdução à Lógica Digital

**Implementação otimizada
de funções lógicas
(continuação)**

Prof. Vanderlei Bonato

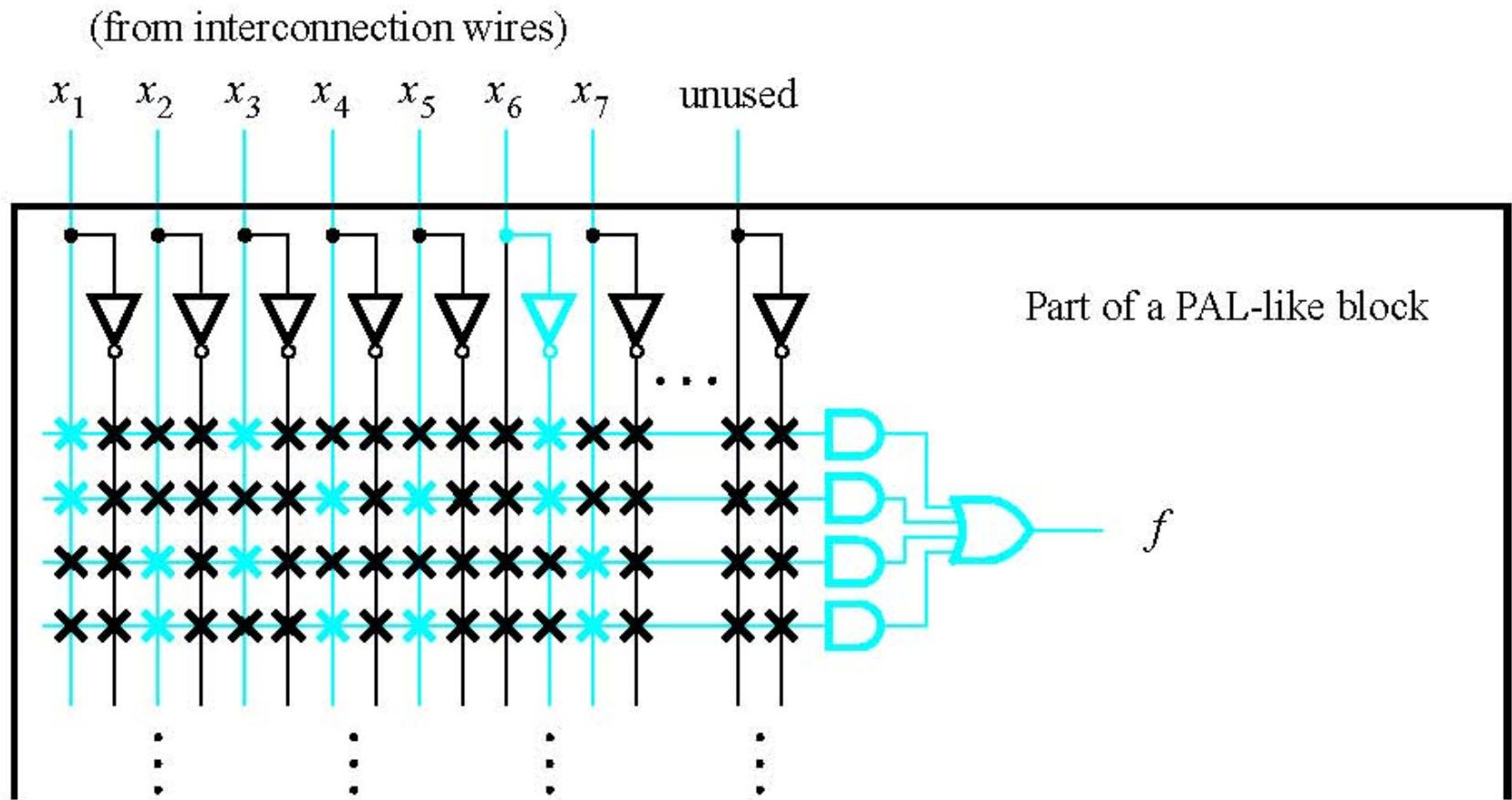


Figure 4.18. Implementation in a CPLD.

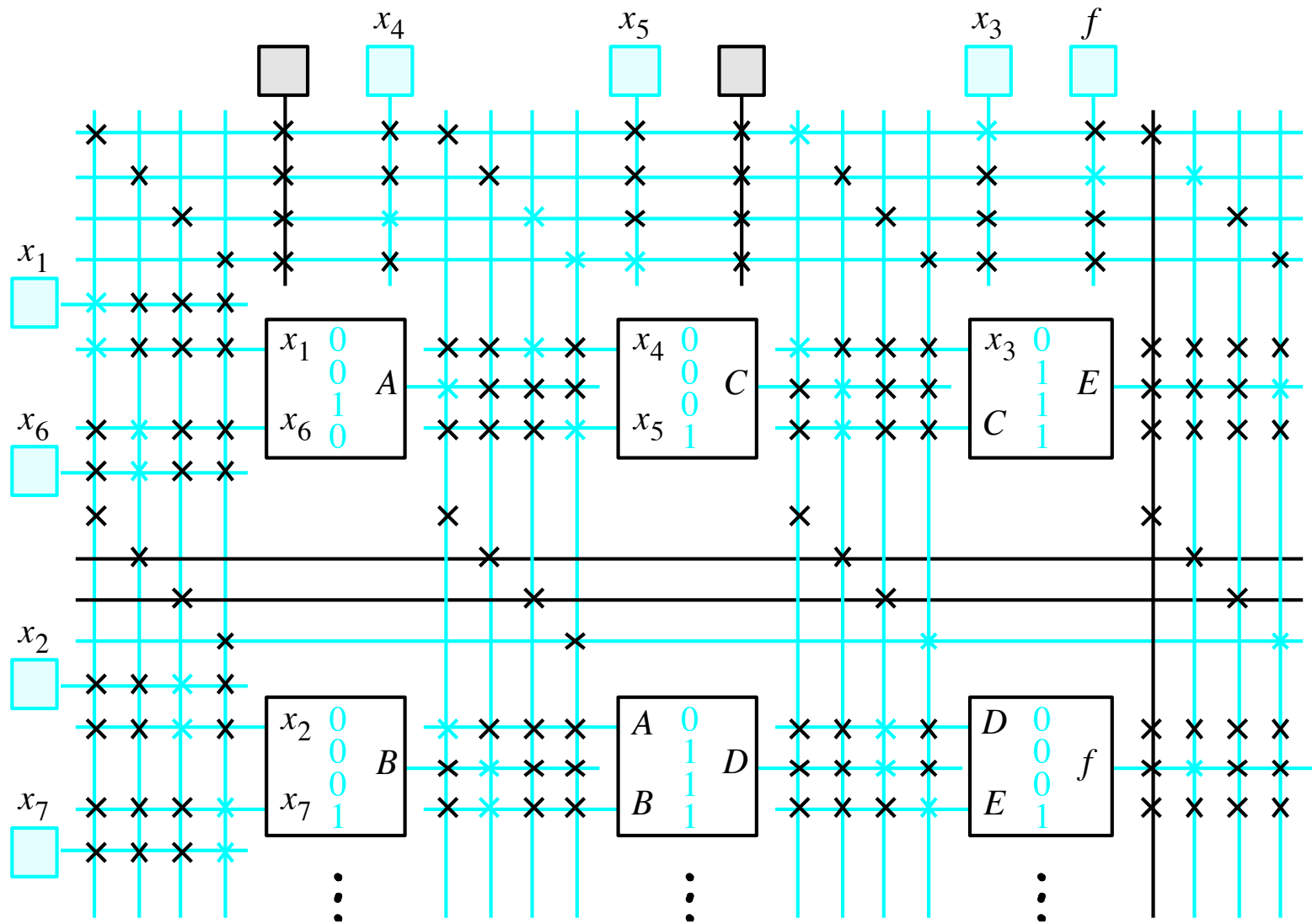


Figure 4.19. Implementation in an FPGA.

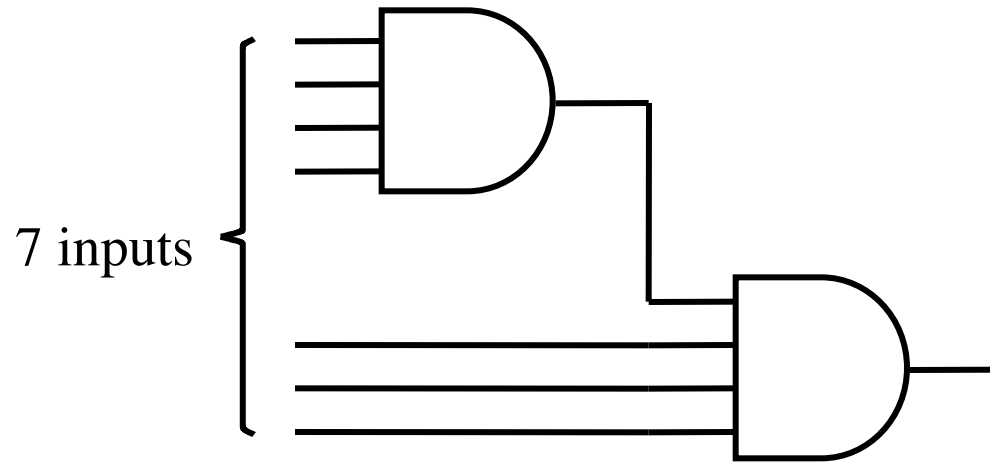


Figure 4.20. Using four-input AND gates to realize a seven-input product term.

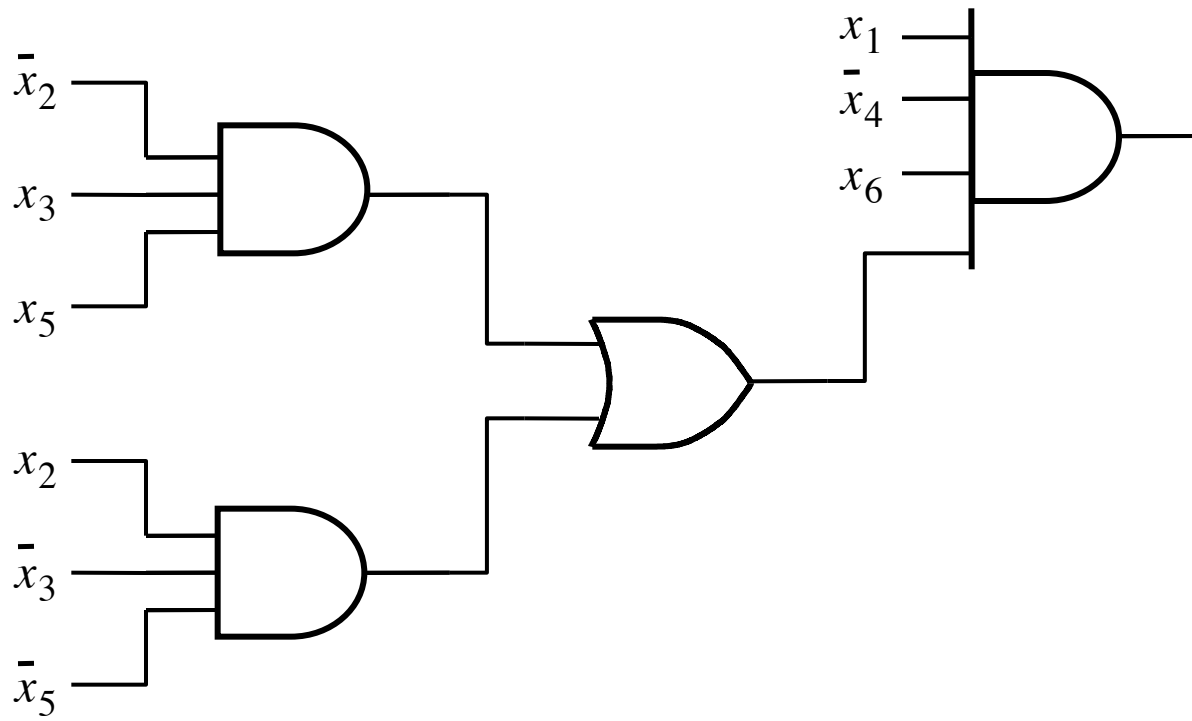


Figure 4.21. A factored circuit.

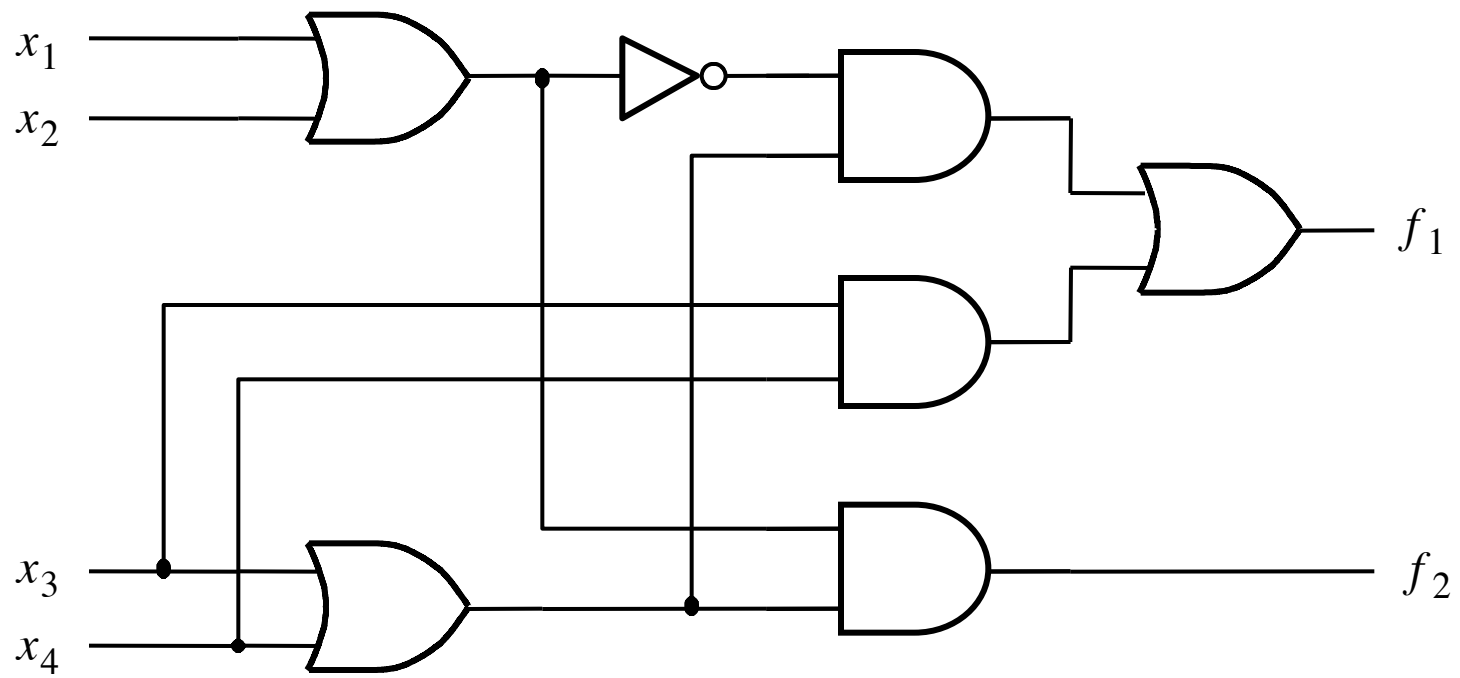


Figure 4.22. Circuit for Example 4.5.

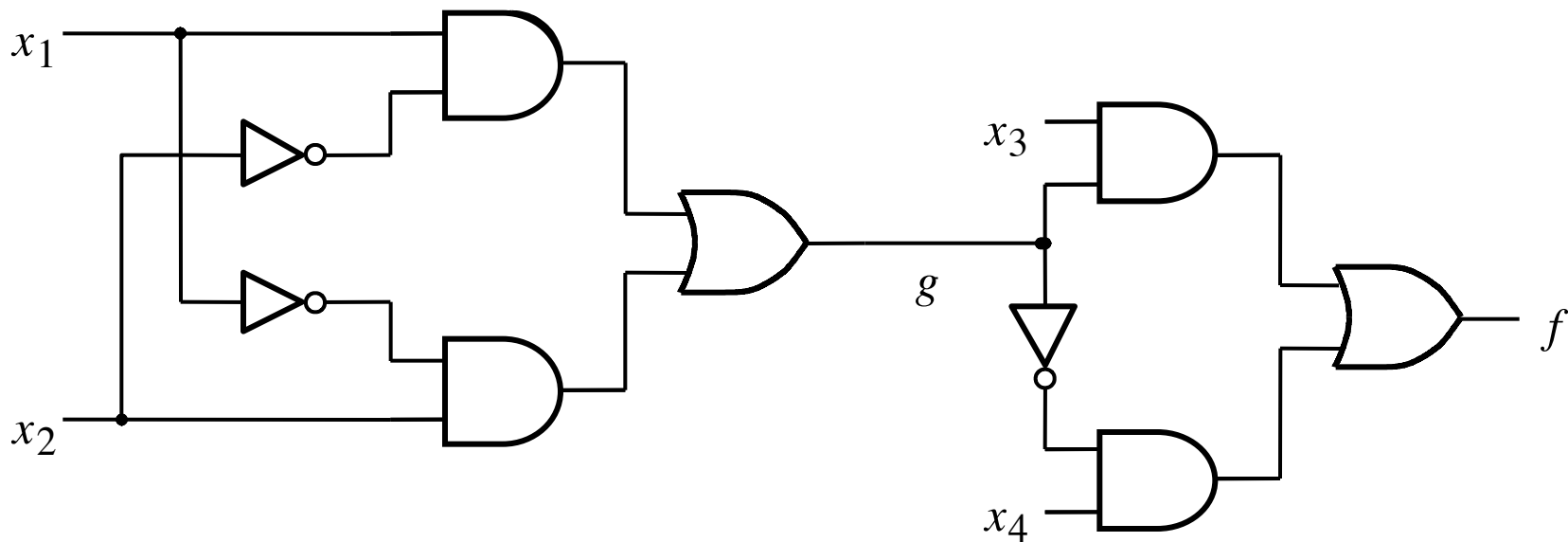


Figure 4.23. Logic circuit for Example 4.6.

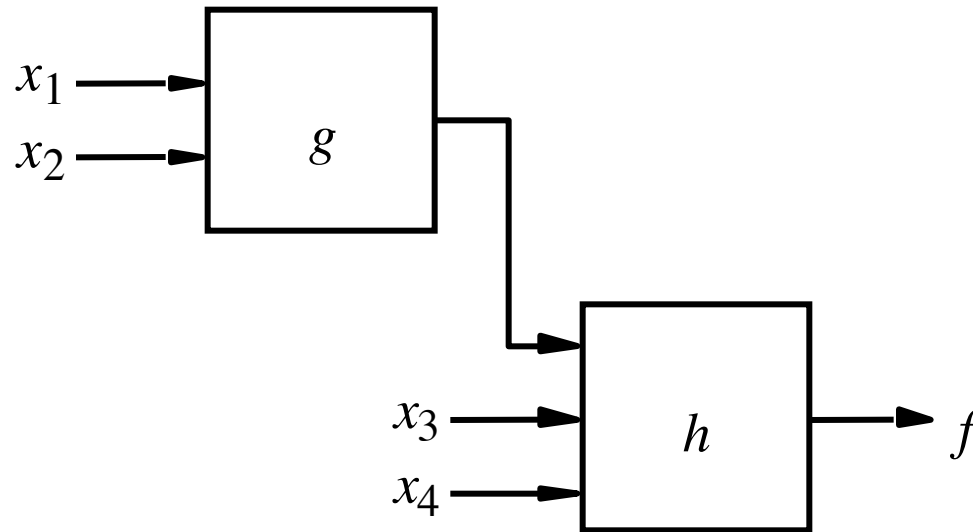
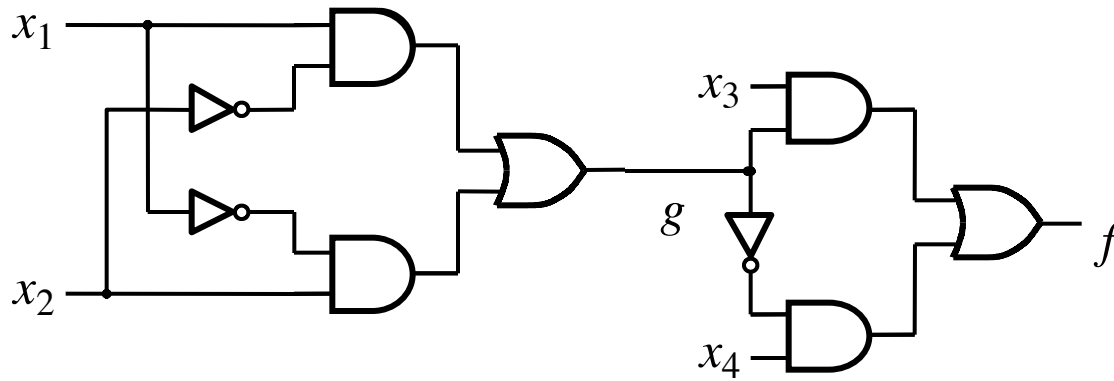


Figure 4.24. The structure of decomposition in Example 4.6.

	$x_1 x_2$			
$x_3 x_4$	00	01	11	10
00	1			
01	1	1	1	1
11	1			
10	1	1	1	1

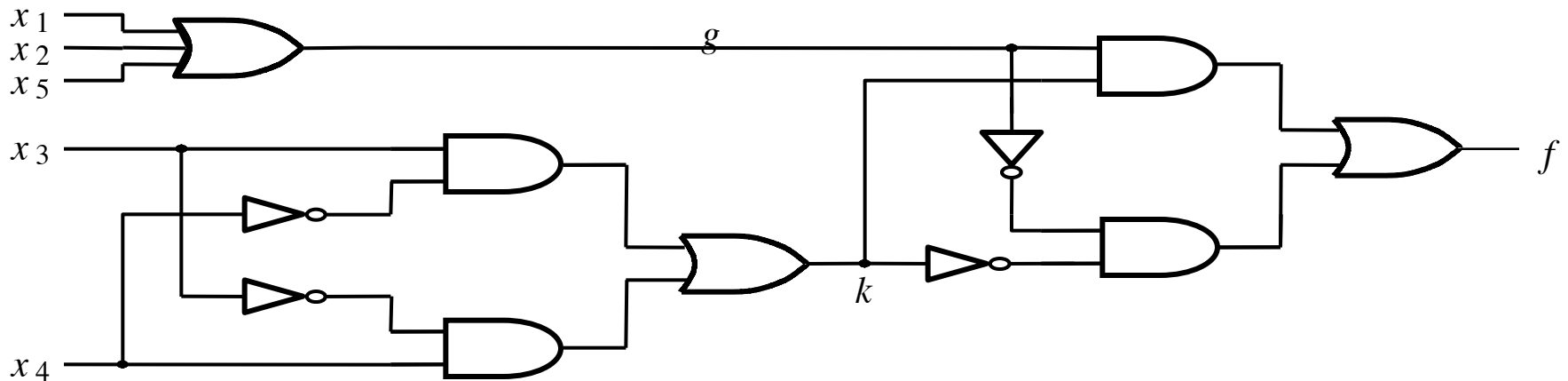
$$x_5 = 0$$

(a) Karnaugh map for the function

	$x_1 x_2$			
$x_3 x_4$	00	01	11	10
00				
01	1	1	1	1
11				
10	1	1	1	1

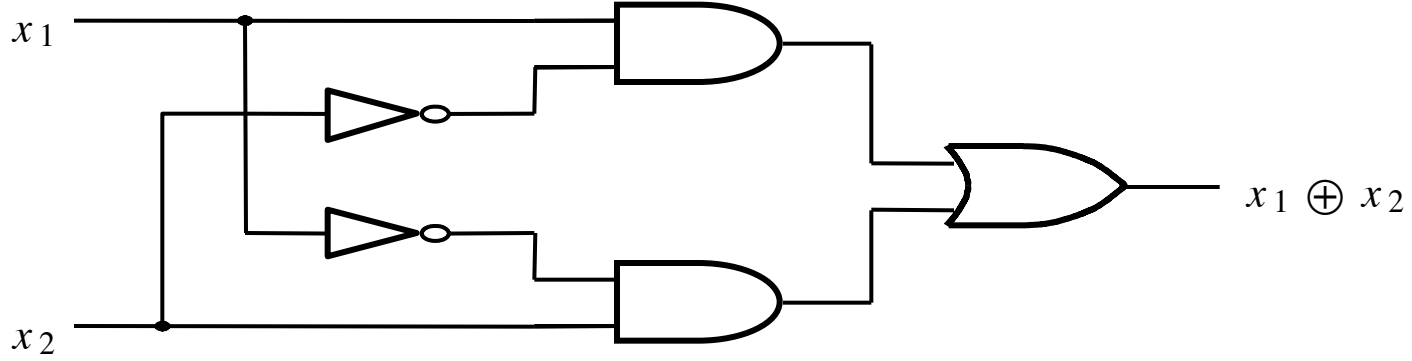
$$x_5 = 1$$

f

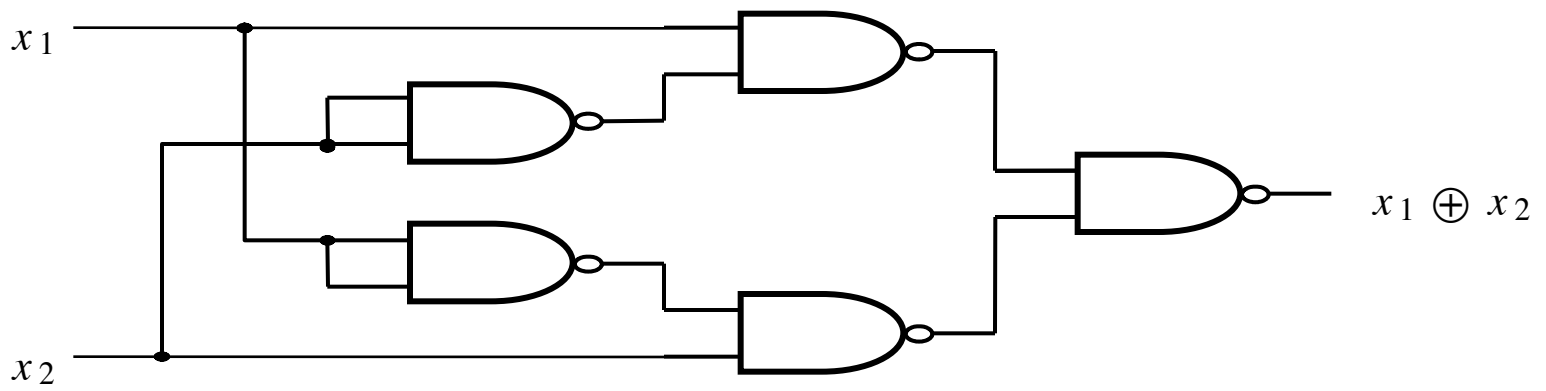


(b) Circuit obtained using decomposition

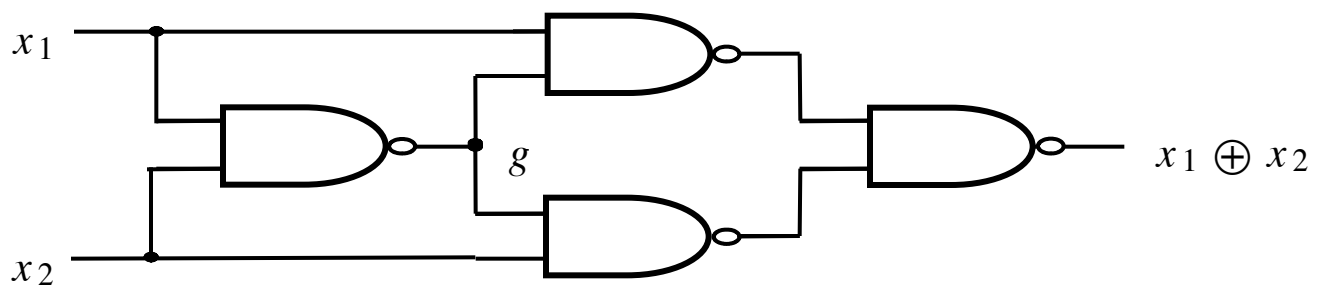
Figure 4.25. Decomposition for Example 4.7.



(a) Sum-of-products implementation

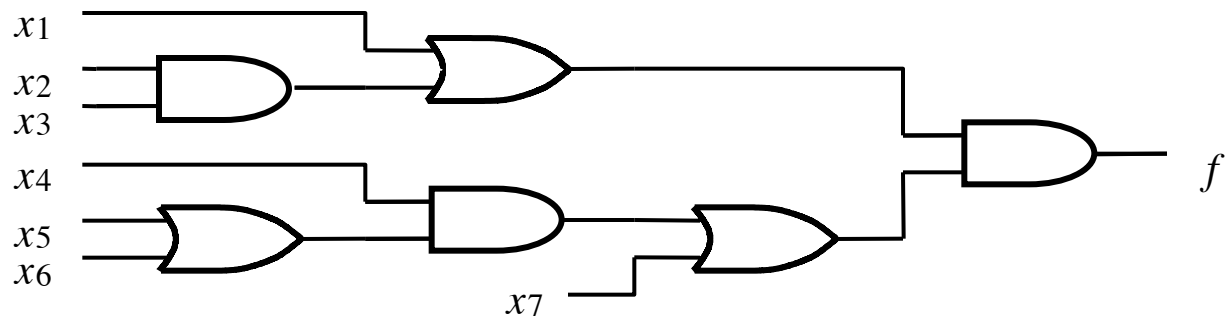


(b) NAND gate implementation

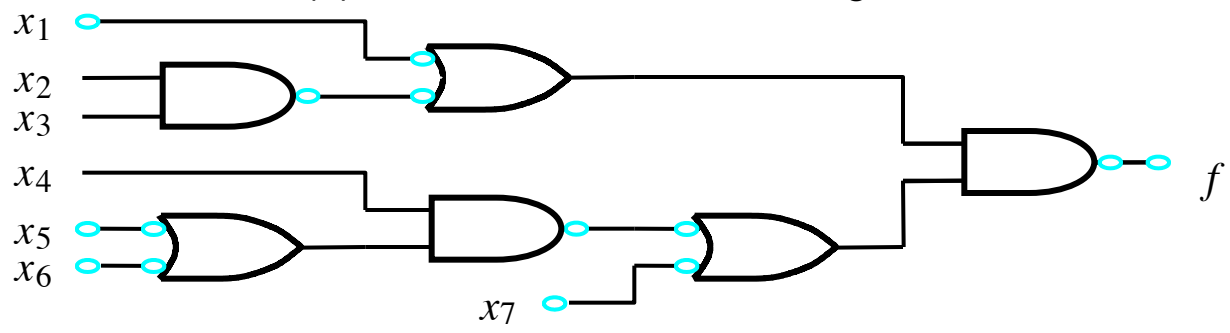


(c) Optimal NAND gate implementation

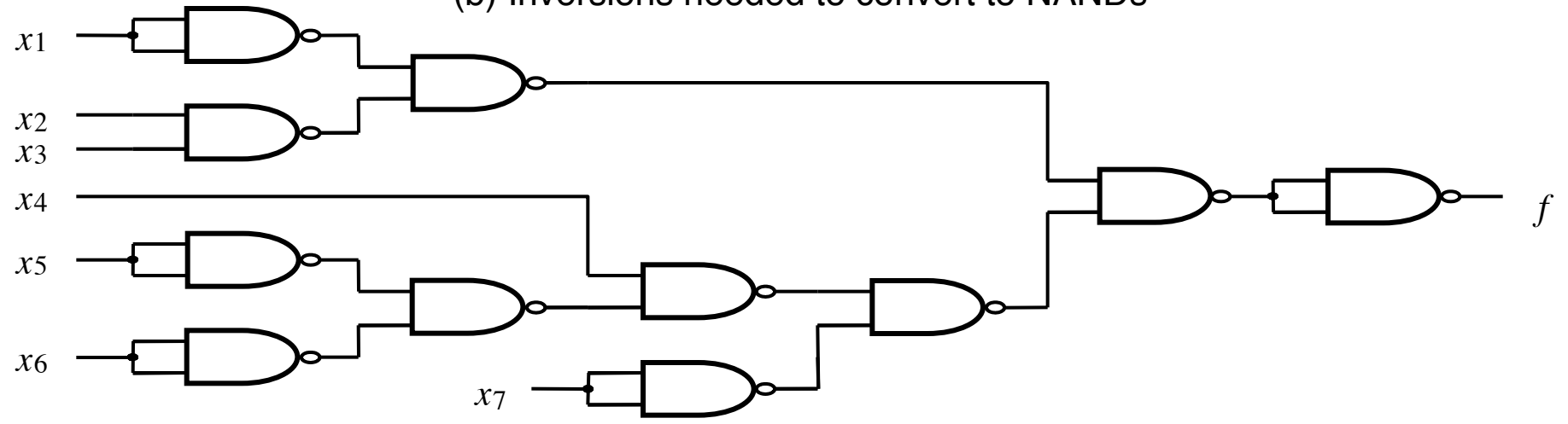
Figure 4.26. Implementation of XOR.



(a) Circuit with AND and OR gates

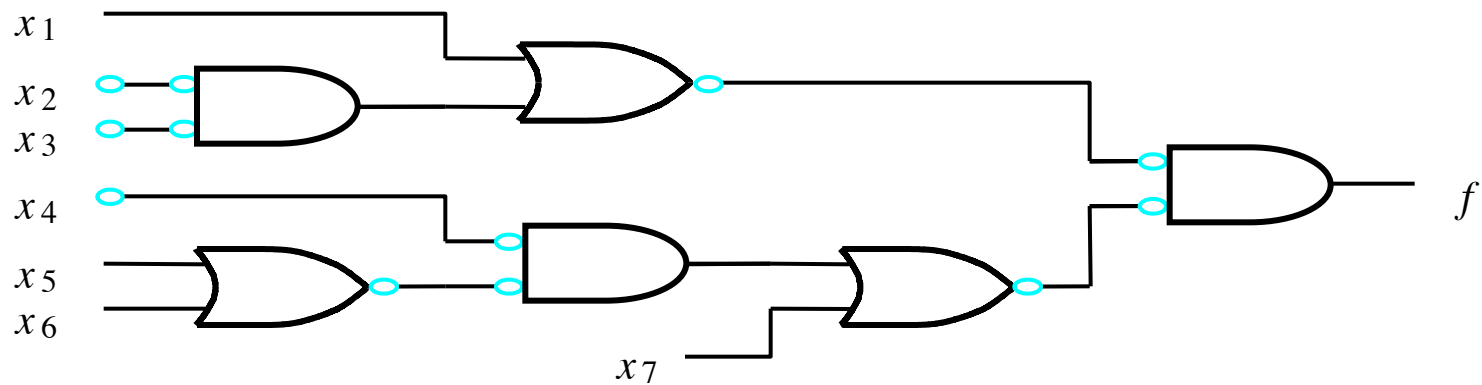


(b) Inversions needed to convert to NANDs

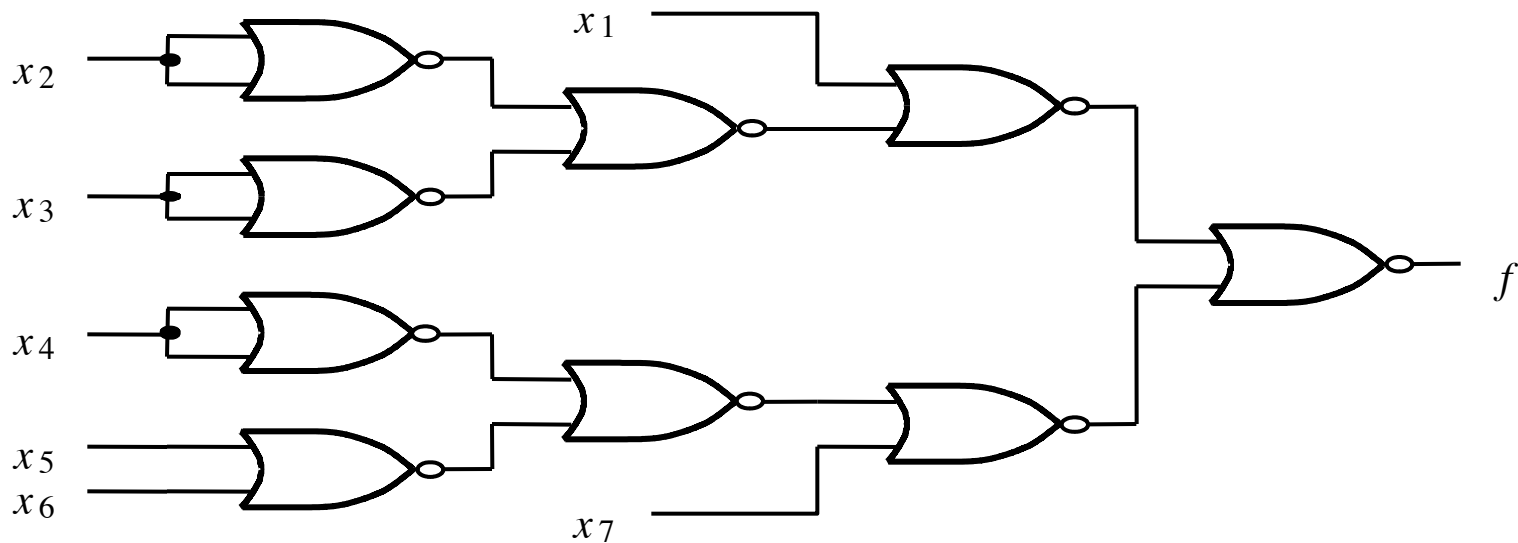


(c) NAND-gate circuit

Figure 4.27. Conversion to a NAND-gate circuit.



(a) Inversions needed to convert to NORs



(b) NOR-gate circuit

Figure 4.28. Conversion to a NOR-gate circuit.

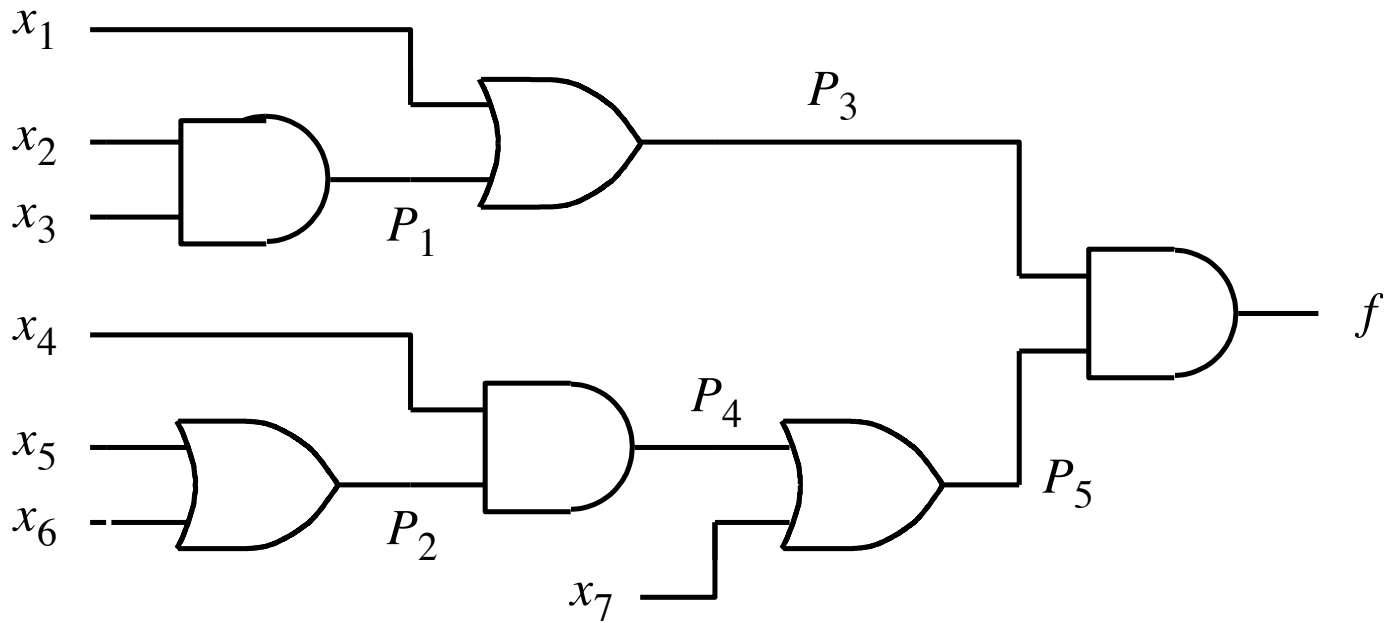


Figure 4.29. Circuit for Example 4.10.

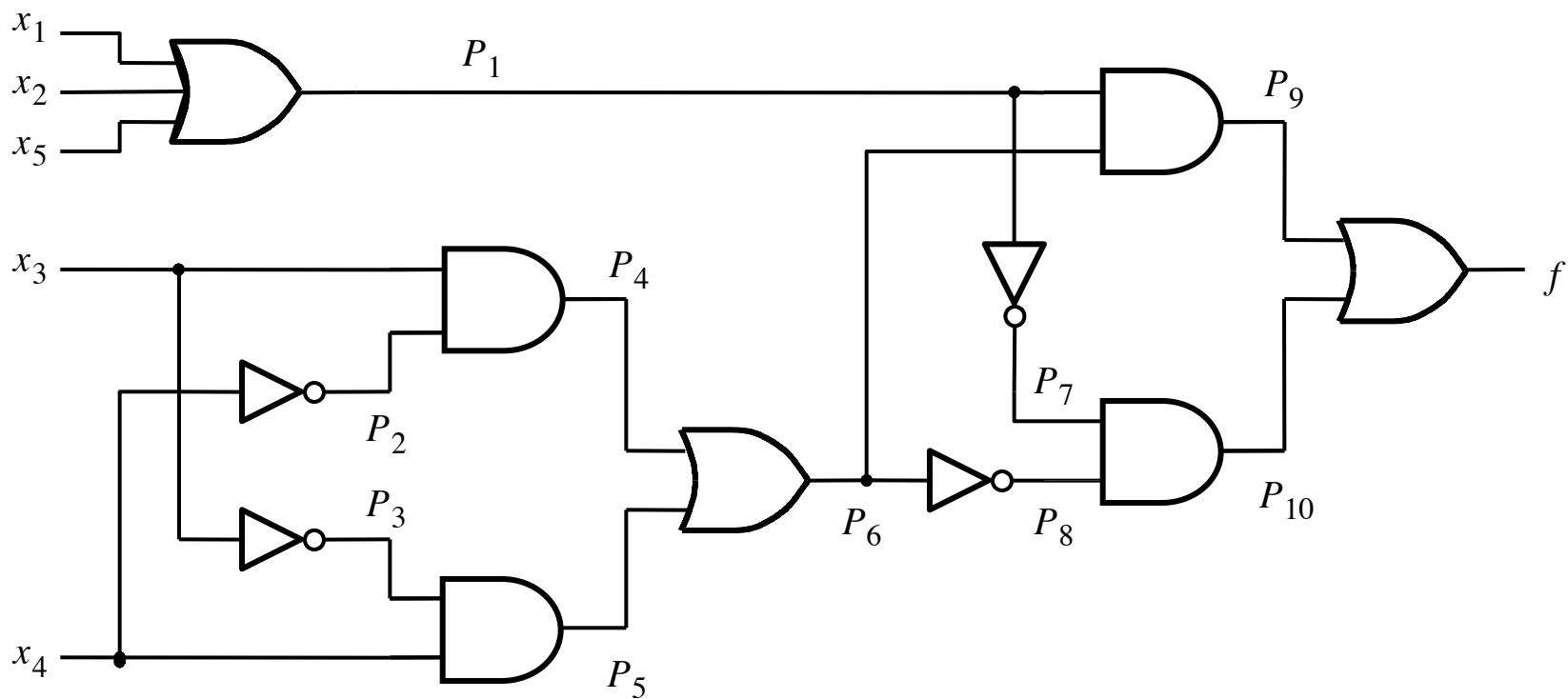
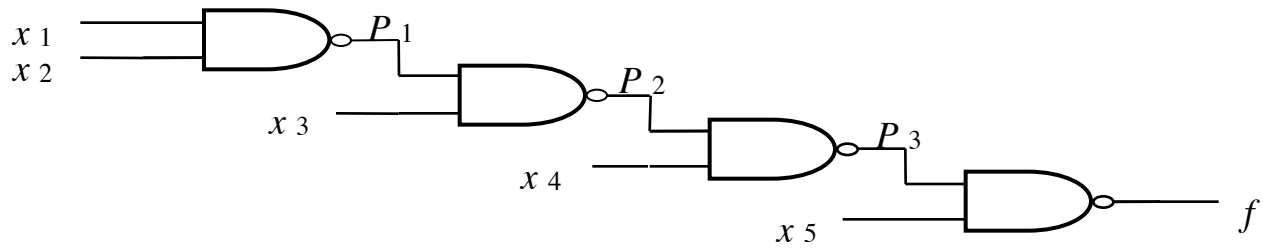
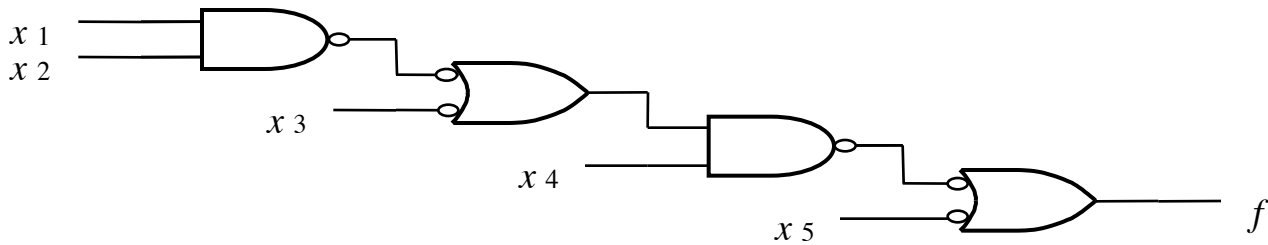


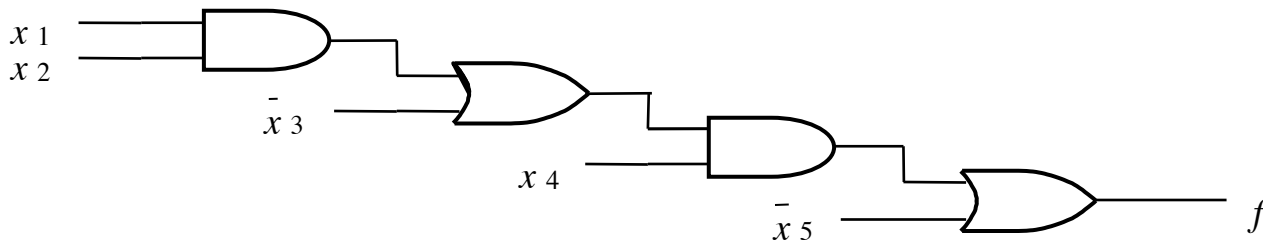
Figure 4.30. Circuit for Example 4.11.



(a) NAND-gate circuit



(b) Moving bubbles to convert to ANDs and ORs



(c) Circuit with AND and OR gates

Figure 4.31. Circuit for Example 4.12.

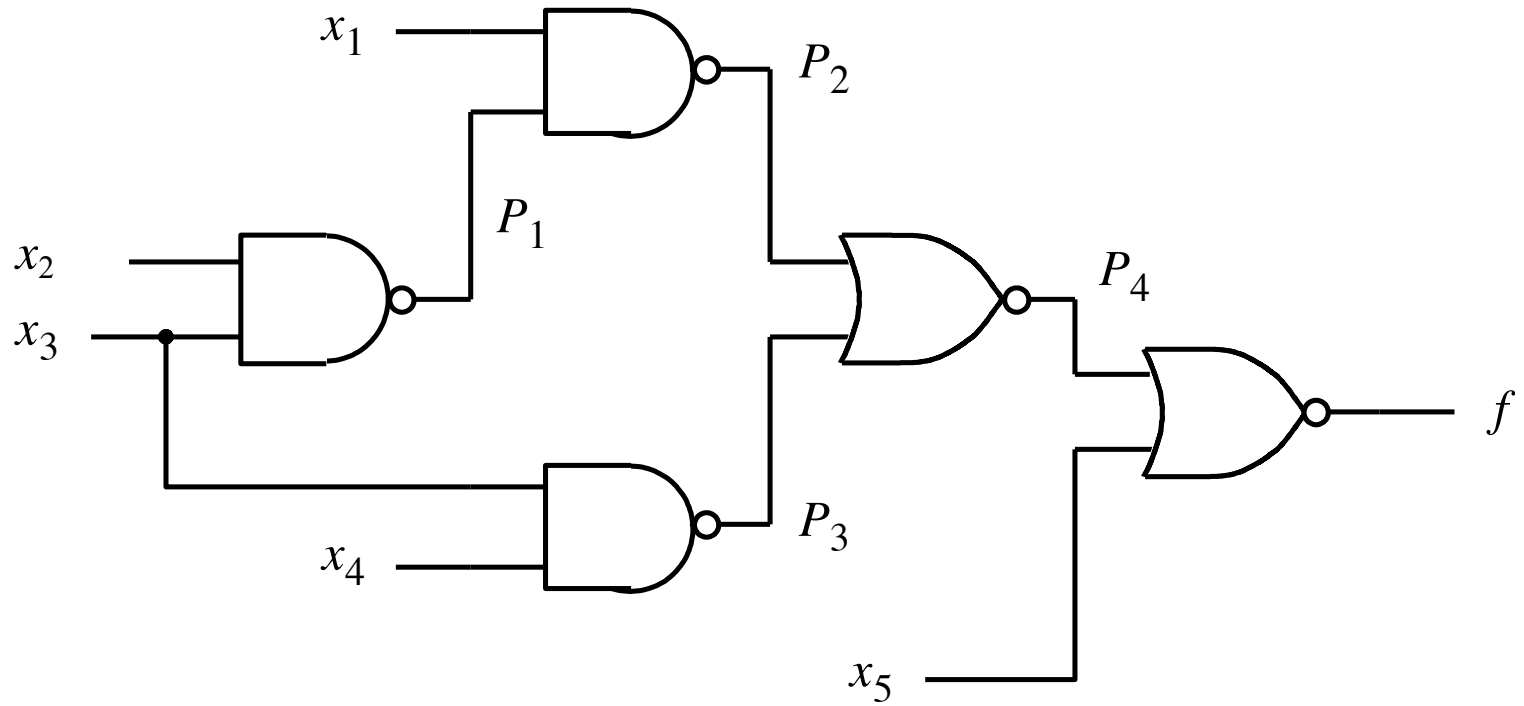


Figure 4.32. Circuit for Example 4.13.