

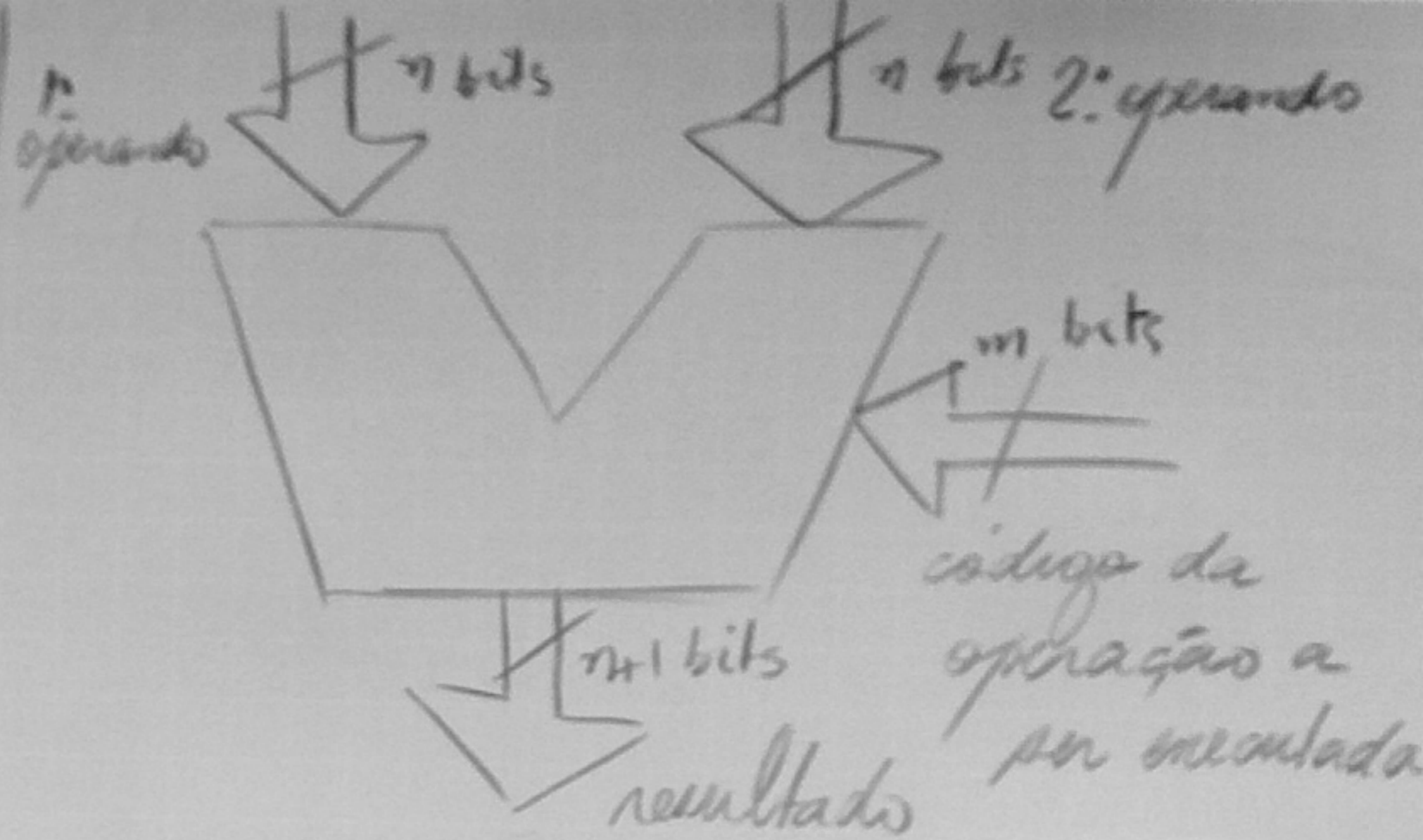
Fla -

Unidade Lógica e Aritmética

Na arquitetura de um computador,
a ULA é o bloco responsável pela
realização das operações lógicas e
das operações aritméticas.

As ALUs mais simples são circuitos combinacionais que aceitam dois operandos, com " n " bits cada um, e um código de operação com " m " bits.

A saída, normalmente, apresenta $n+1$ bits.



Exercício

projetar uma ULA

para dois operandos de

4 bits, com as seguintes

características:

> números com sinal
em complemento de
dois: faixa de
-8 a +7

> funções

• adição de números
com sinal

• subtração de números
com sinal

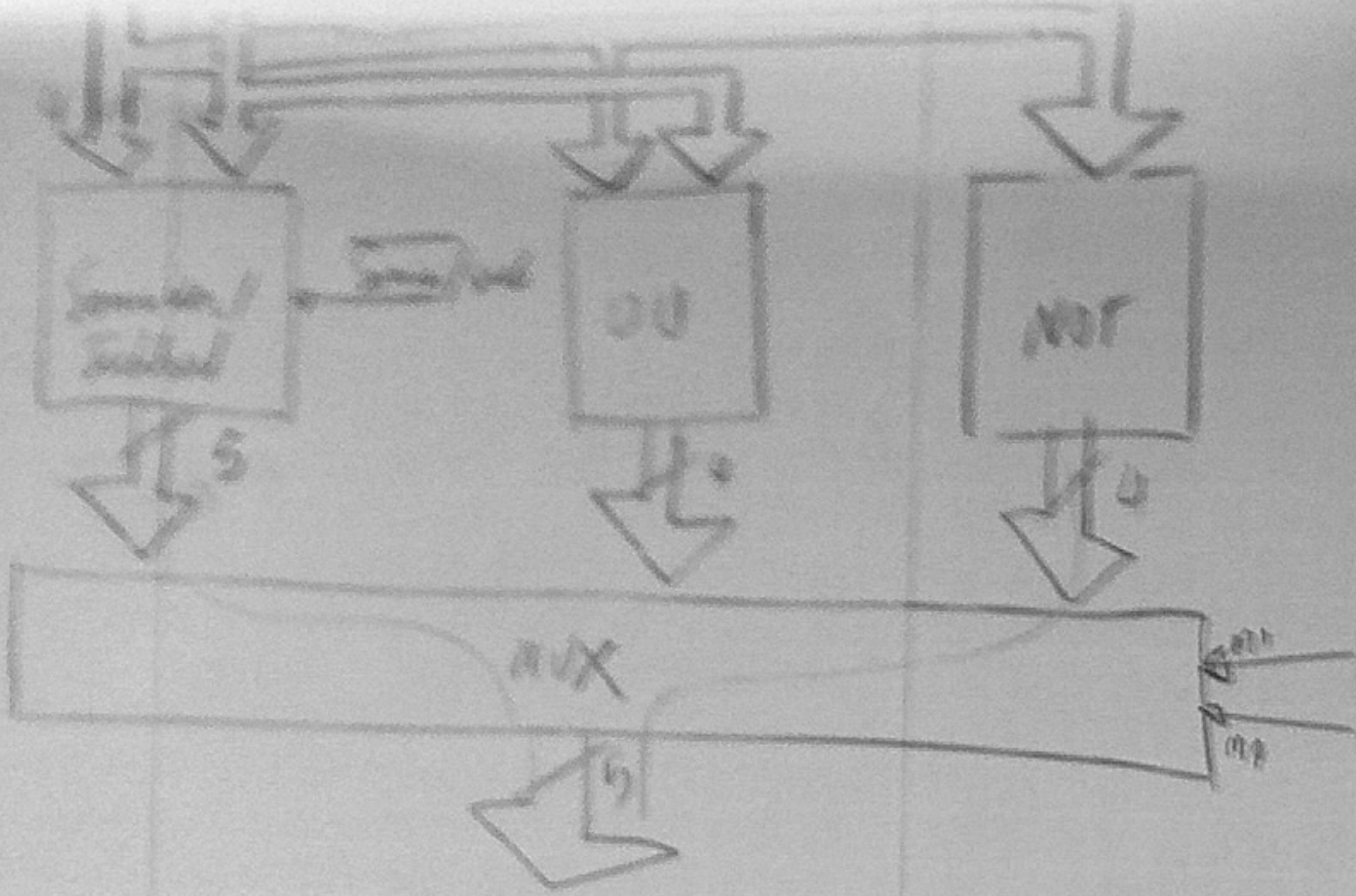
• função OR (4 bits)

• função AND (4 bits)

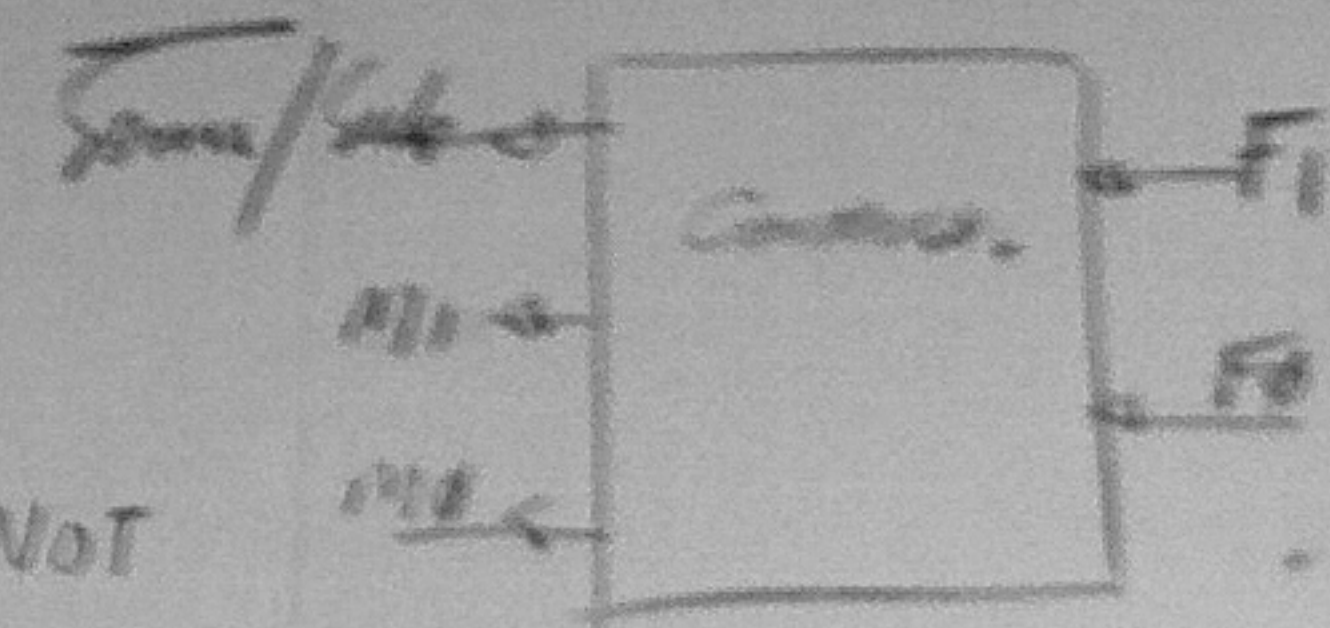
11. ~~...~~ - 4.4.2 - ...

11. ~~...~~ - 4.4.5

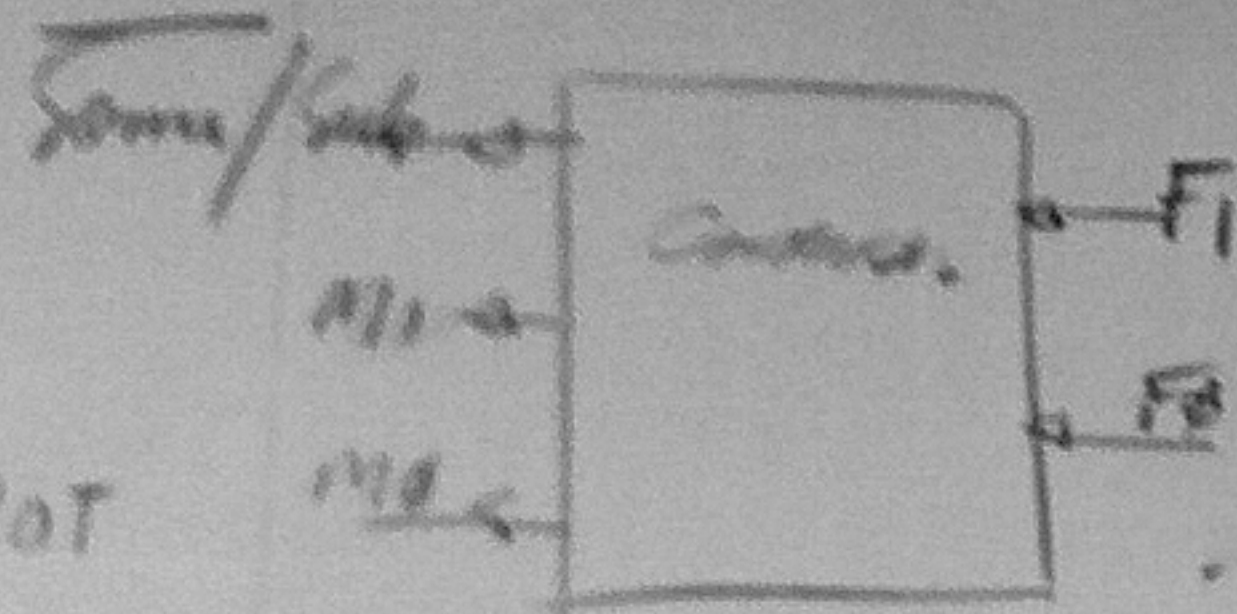
11. ~~...~~
11. ~~...~~
11. ~~...~~
11. ~~...~~



- Control
- $\phi\phi \rightarrow$ NOT
 - $01 \rightarrow$ 00
 - $10 \rightarrow$ Sum/Sub

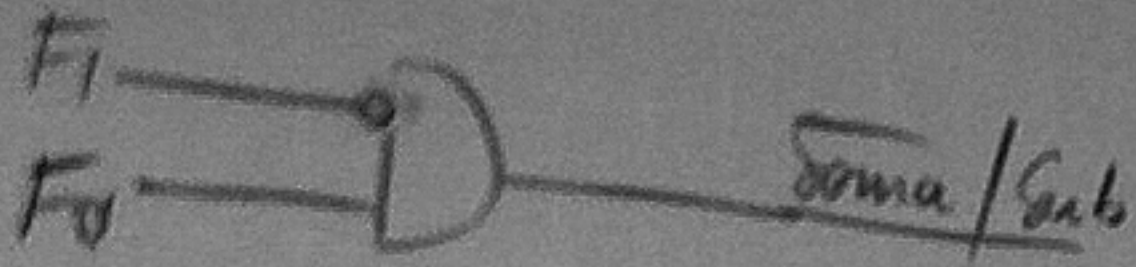


- NOT
- OU
- Sum/Sub



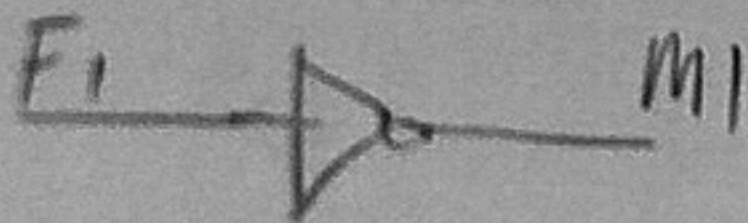
F ₁	F ₀	S ₁ /S ₀	A ₁	A ₀	
0	0	0	1	0	Suma
0	1	1	1	0	Sub
1	0	X	0	1	OU
1	1	X	0	0	NOT

Conversion

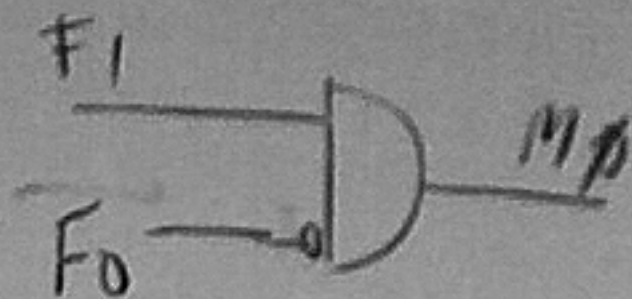


$$M_1 = \bar{F}_1 \bar{F}_0 + \bar{F}_1 F_0 = \bar{F}_1 (F_0 + \bar{F}_0)$$

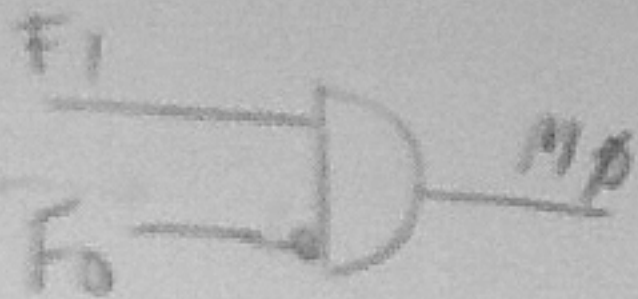
$$M_1 = \bar{F}_1$$



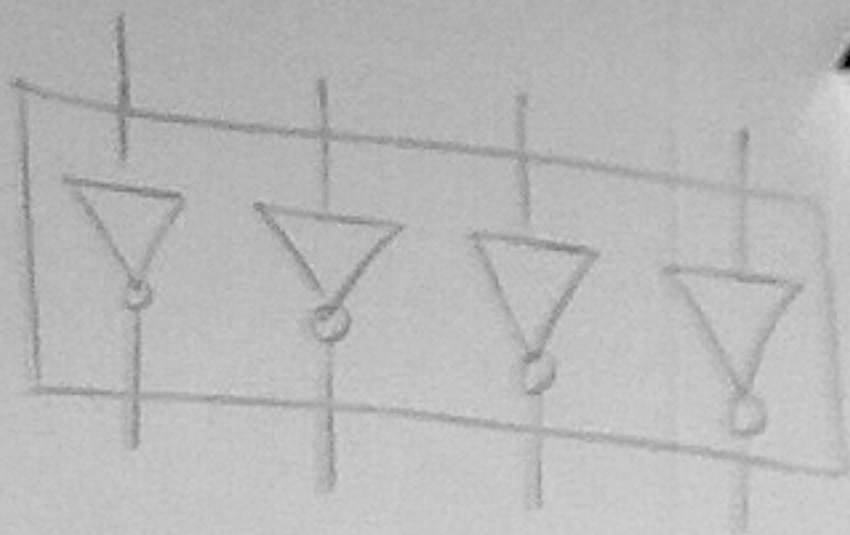
$$M_0 = F_1 \bar{F}_0$$



$$M_0 = F_1 \overline{F_0}$$

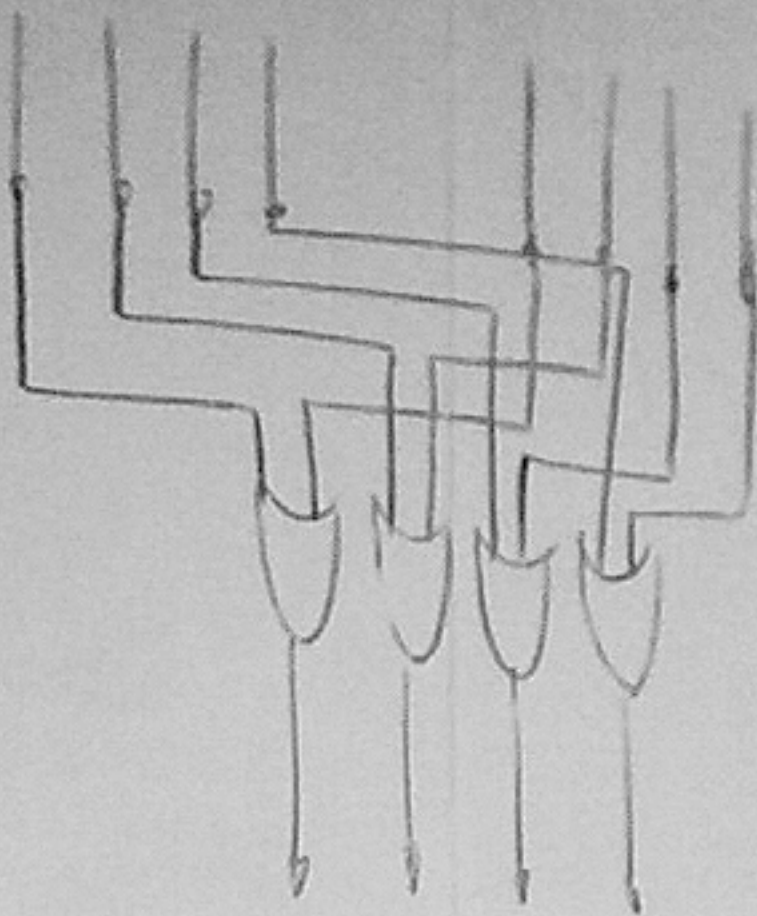


How
NOT



Plano

DU



Sumator / Subtrator Z_1

$$A \cdot B \quad \text{---} \quad A + B$$

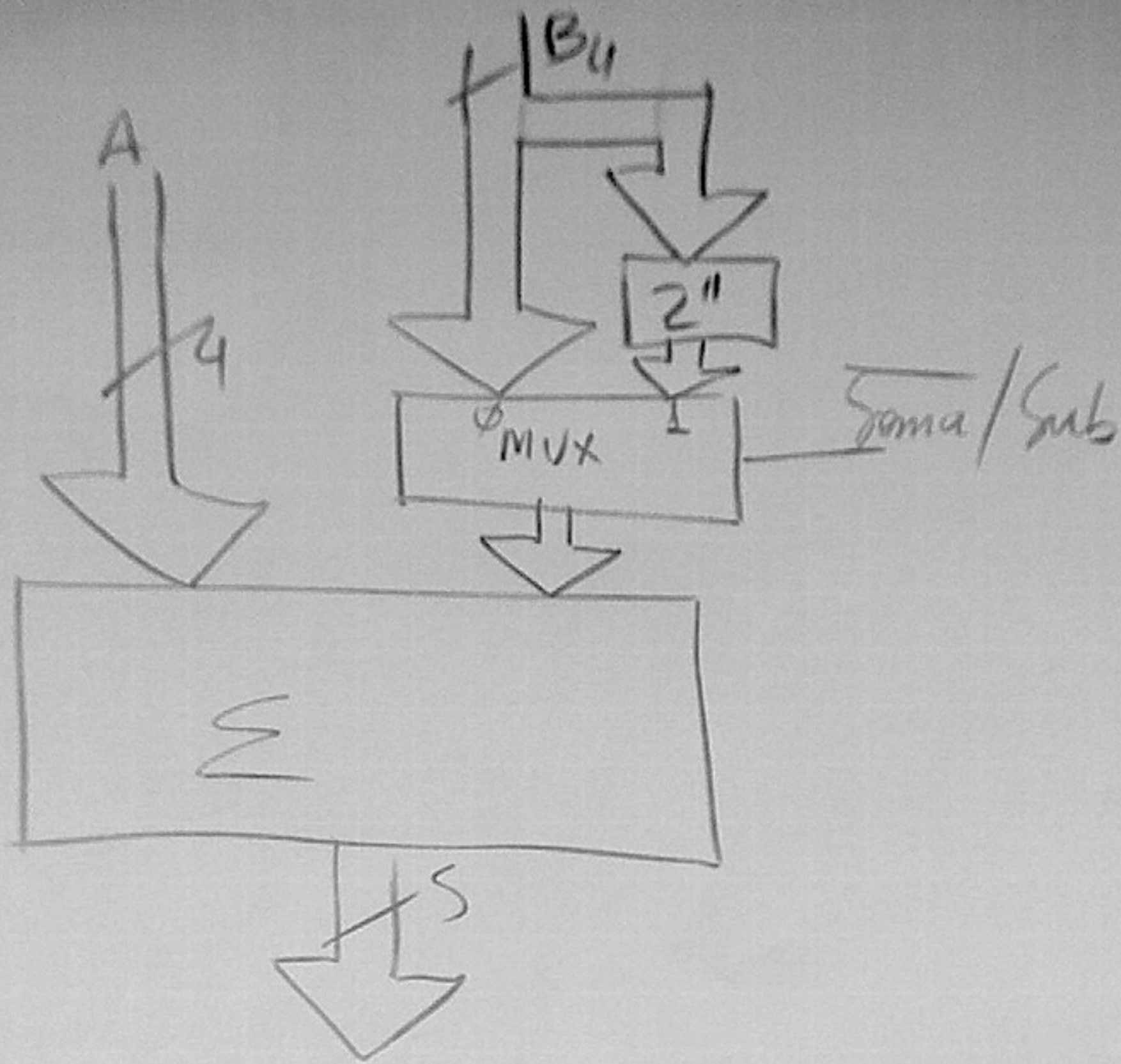
$$A \cdot B \quad \text{---} \quad A + B''$$

⊕

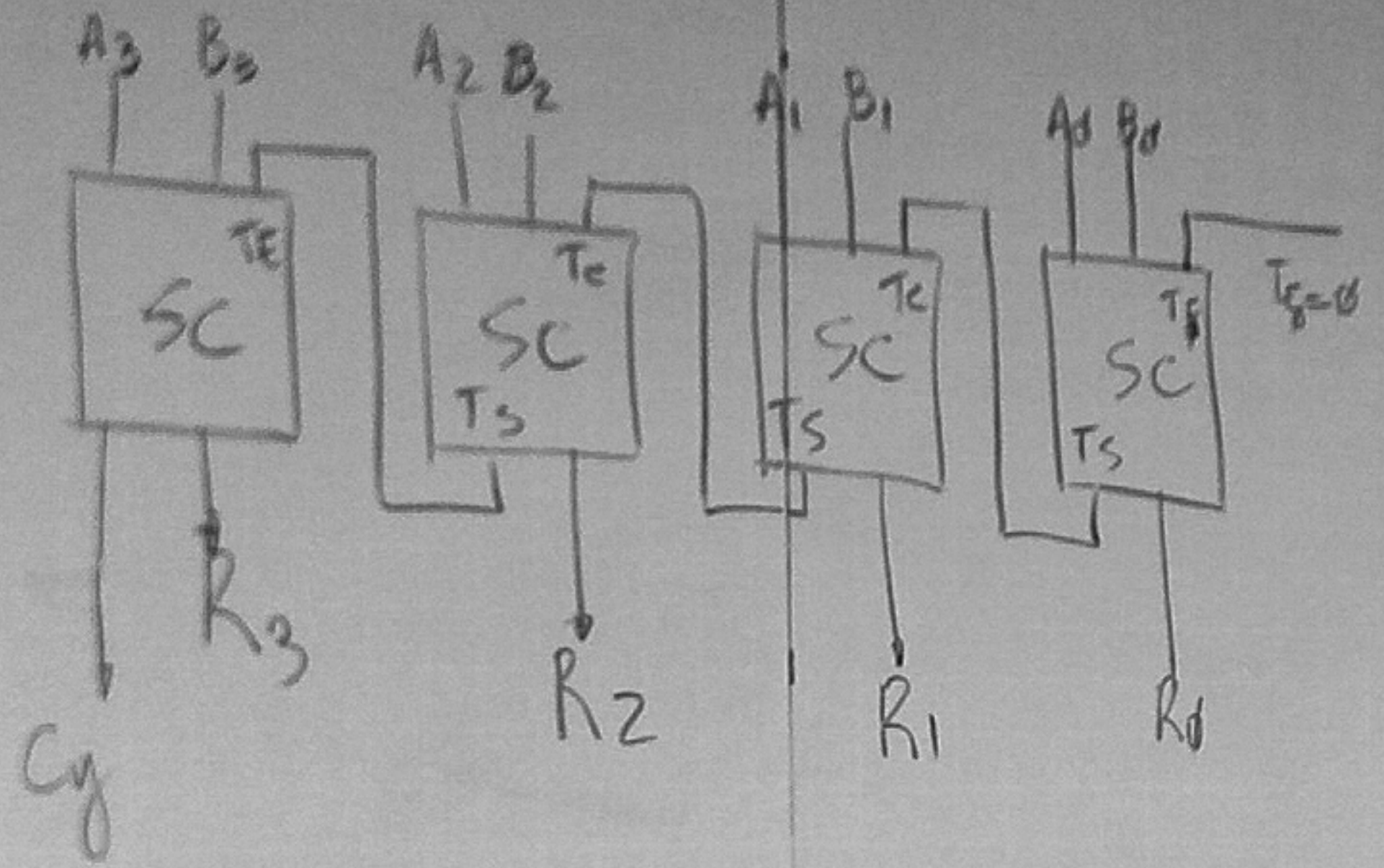
⊖

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

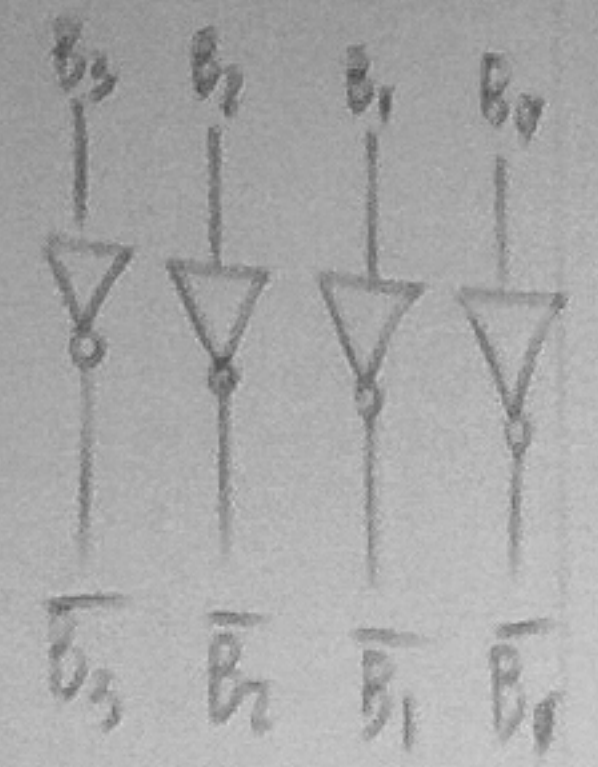
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0



Block Σ

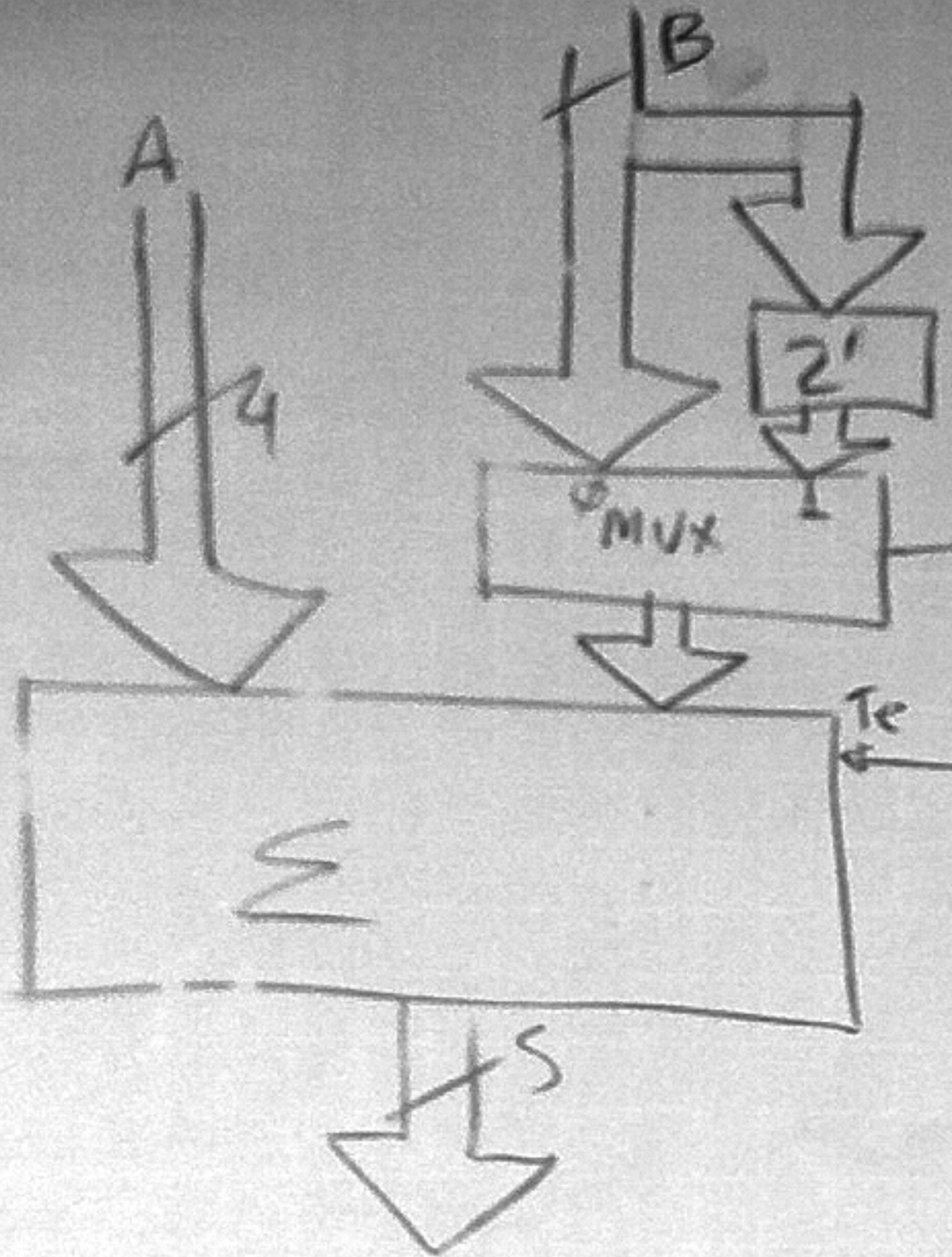


2''



$T_3 = 1$

Total sum/outs



A 0111 \rightarrow +7
 B 1010 \rightarrow -6

A+B \rightarrow

0111	
1010	
X0001	

A-B