SCE 0117 - Introdução à Lógica Digital

Introdução aos circuitos lógicos (continuação)

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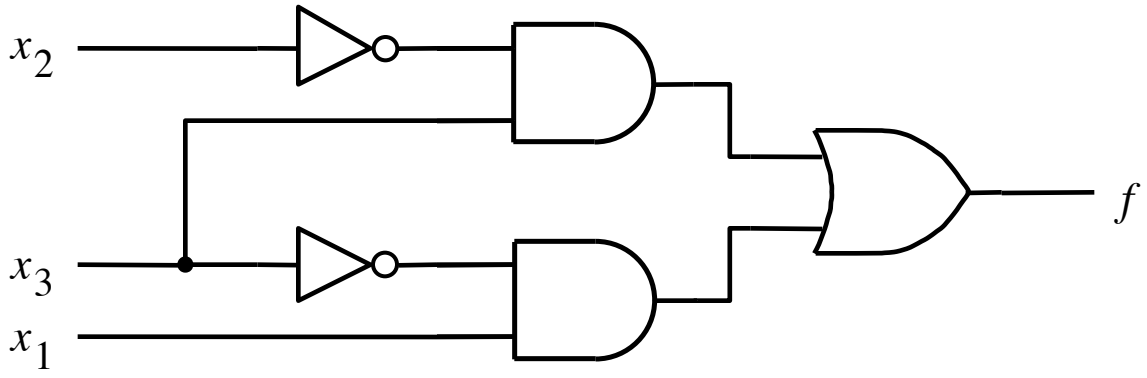
Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \overline{x}_1\overline{x}_2\overline{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \overline{x}_1\overline{x}_2x_3$	$M_1 = x_1 + x_2 + \overline{x}_3$
2	0	1	0	$m_2 = \overline{x}_1x_2\overline{x}_3$	$M_2 = x_1 + \overline{x}_2 + x_3$
3	0	1	1	$m_3 = \overline{x}_1x_2x_3$	$M_3 = x_1 + \overline{x}_2 + \overline{x}_3$
4	1	0	0	$m_4 = x_1\overline{x}_2\overline{x}_3$	$M_4 = \overline{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1\overline{x}_2x_3$	$M_5 = \overline{x}_1 + x_2 + \overline{x}_3$
6	1	1	0	$m_6 = x_1x_2\overline{x}_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$
7	1	1	1	$m_7 = x_1x_2x_3$	$M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

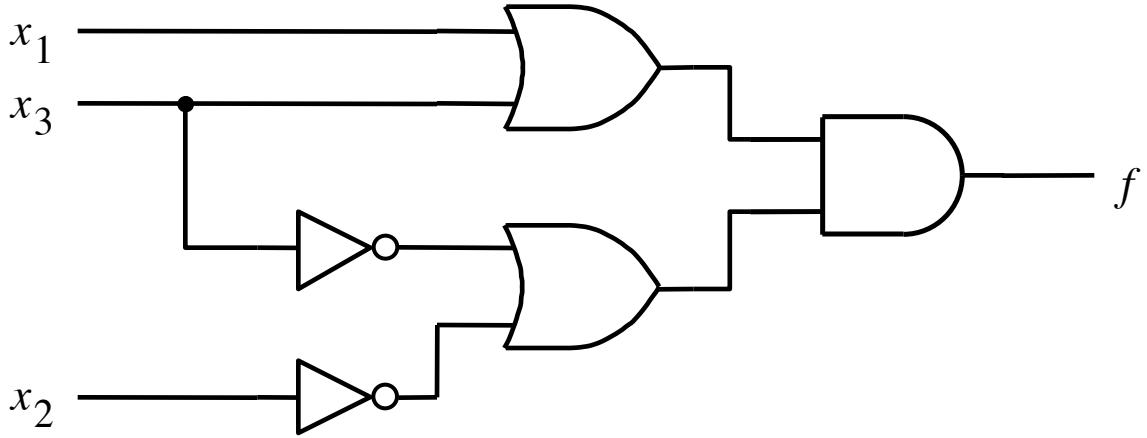
Figure 2.17 Three-variable minterms and maxterms.

Row number	x_1	x_2	x_3	$f(x_1, x_2, x_3)$
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

Figure 2.18. A three-variable function.



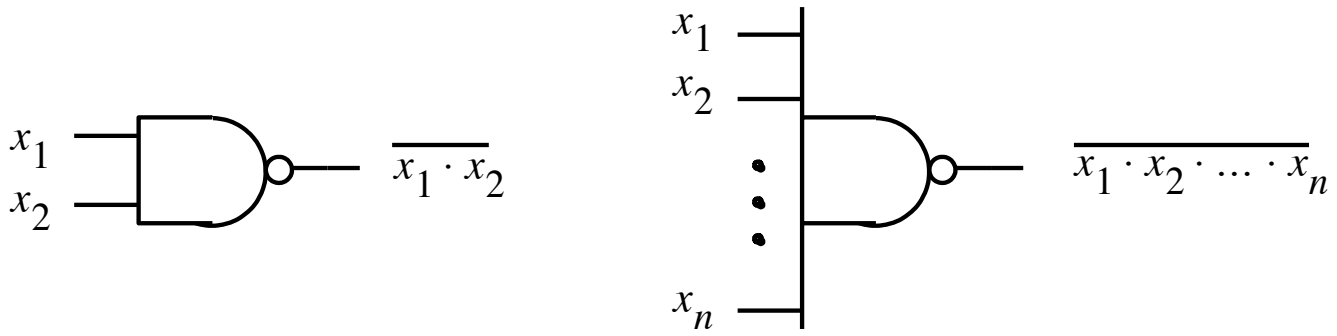
(a) A minimal sum-of-products realization



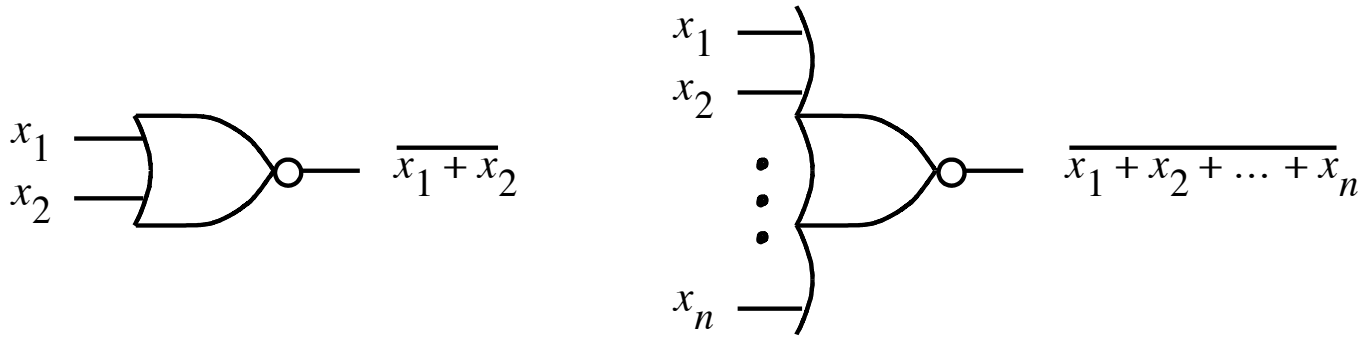
(b) A minimal product-of-sums realization

Figure 2.19. Two realizations of a function in Figure 2.18.

- Estudar os exemplos 2.3 e 2.4

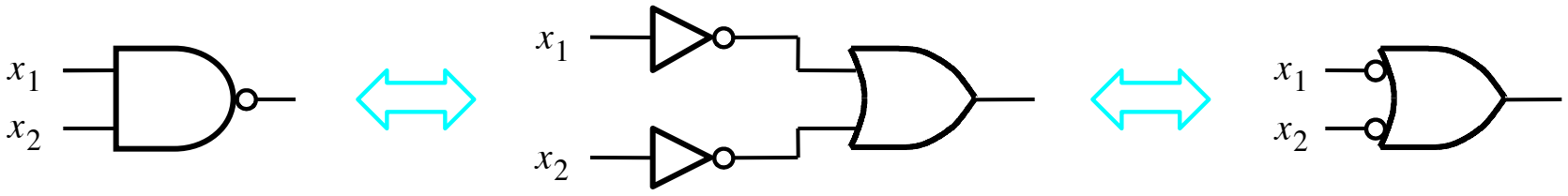


(a) NAND gates

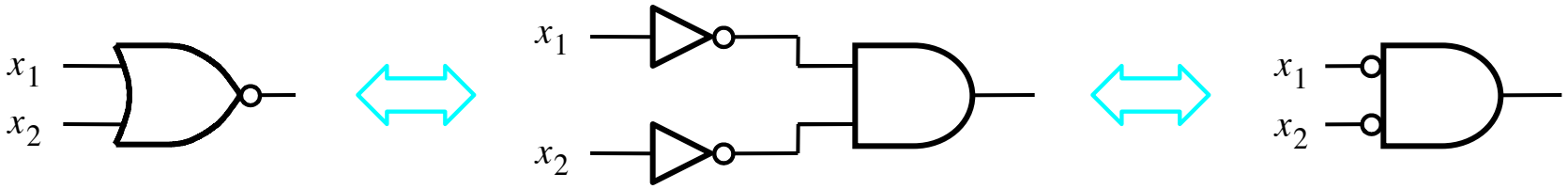


(b) NOR gates

Figure 2.20. NAND and NOR gates.



(a) $\overline{x_1 x_2} = \bar{x}_1 + \bar{x}_2$



(b) $\overline{x_1 + x_2} = \bar{x}_1 \bar{x}_2$

Figure 2.21. DeMorgan's theorem in terms of logic gates.

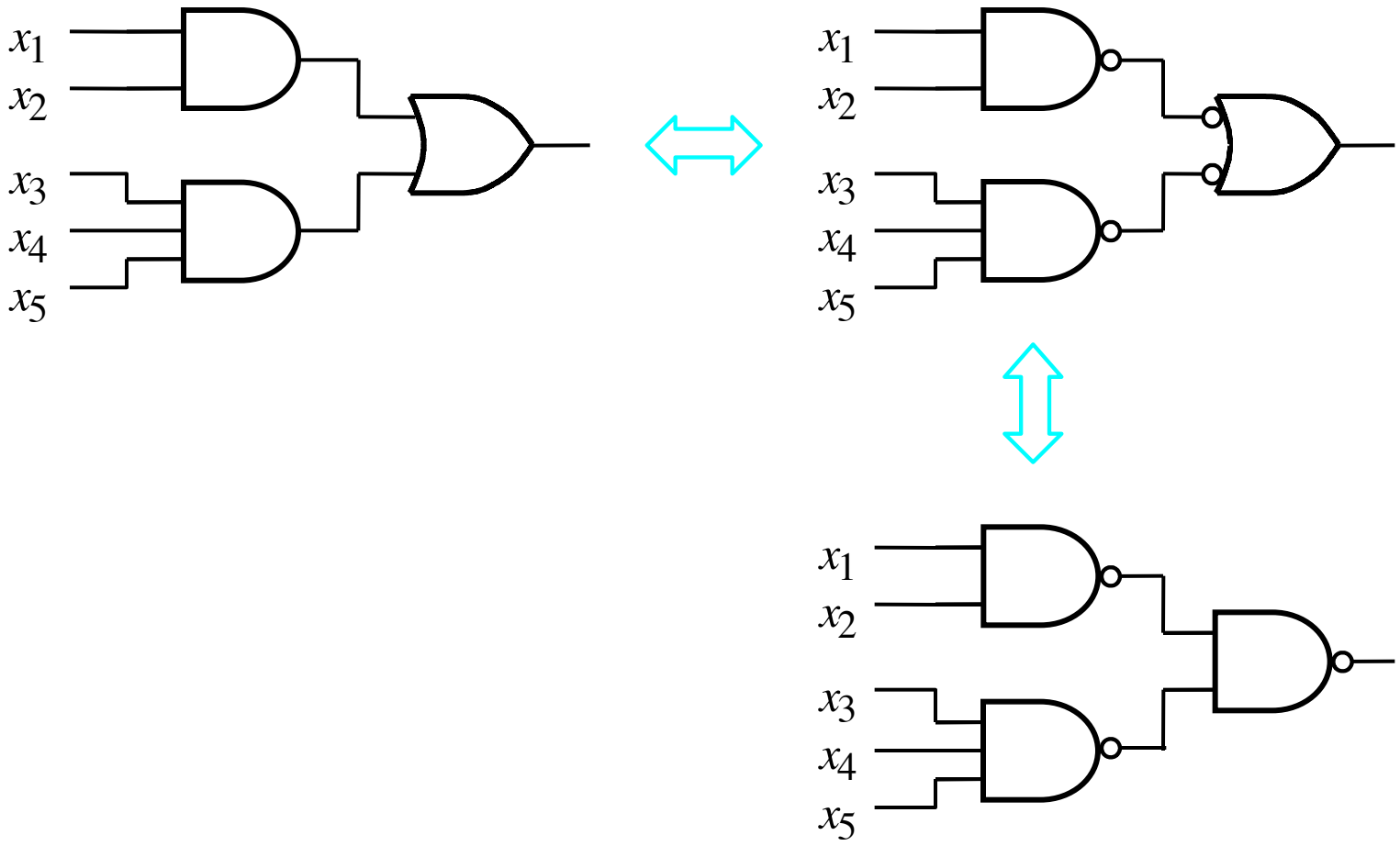


Figure 2.22. Using NAND gates to implement a sum-of-products.

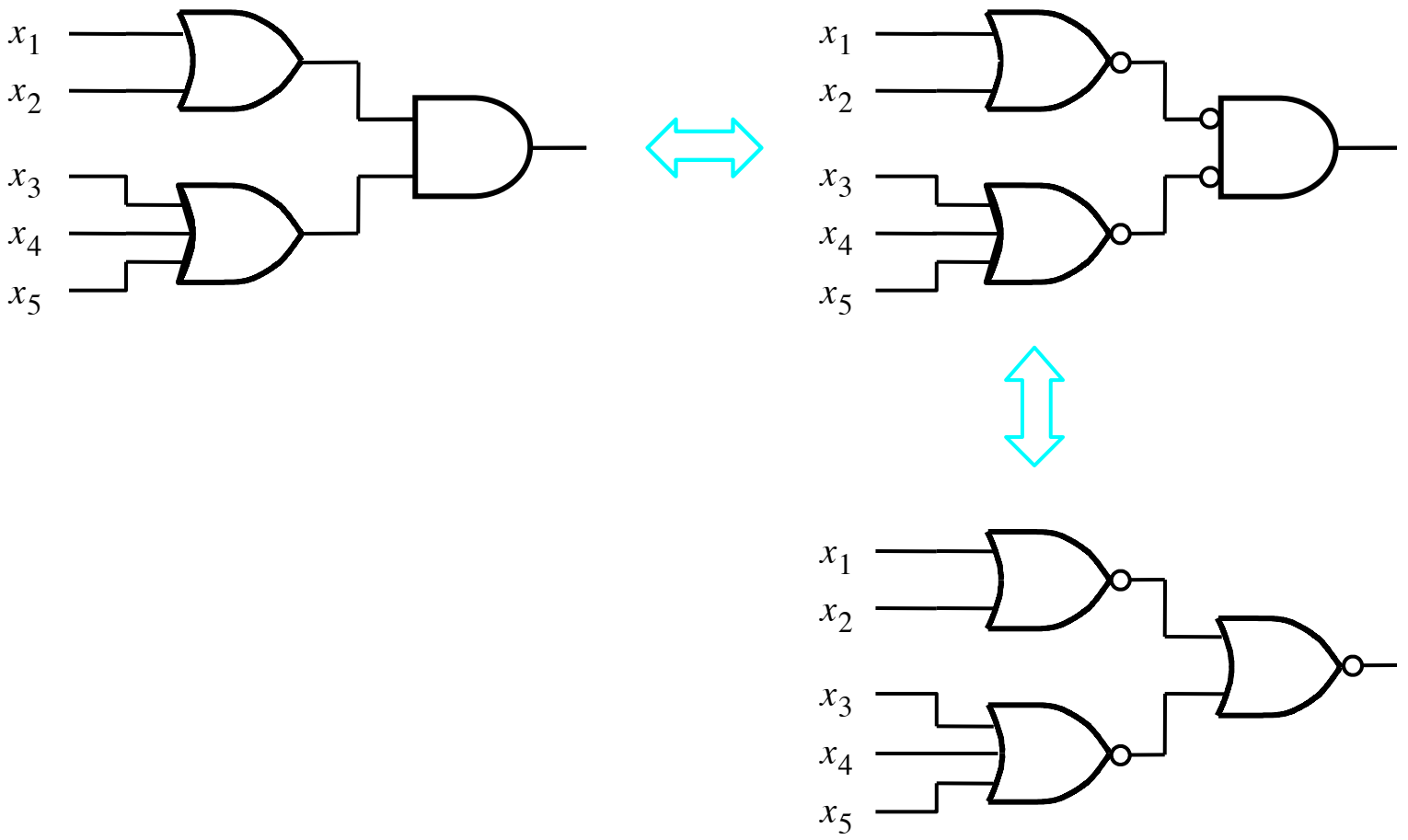
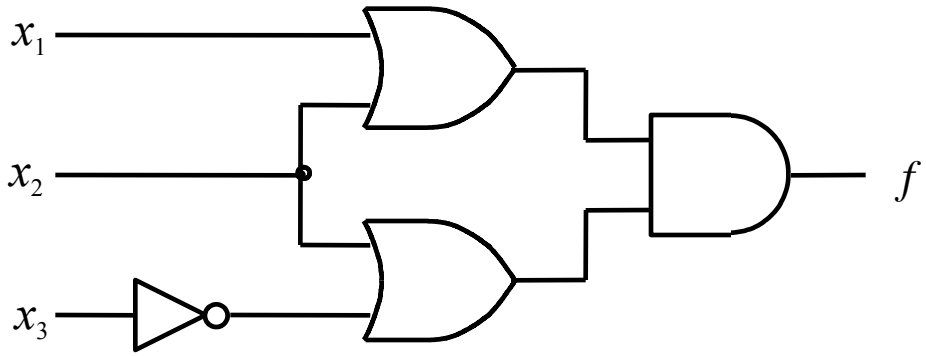
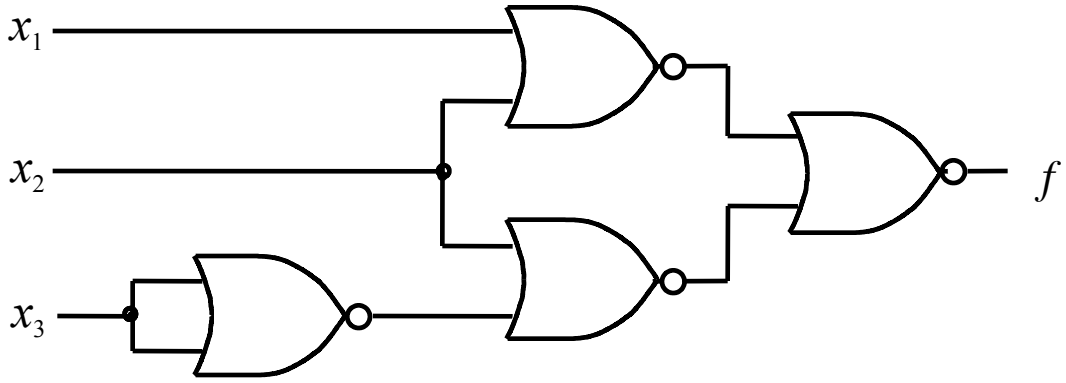


Figure 2.23. Using NOR gates to implement a product-of sums.

- Estudar os exemplos 2.6 e 2.7

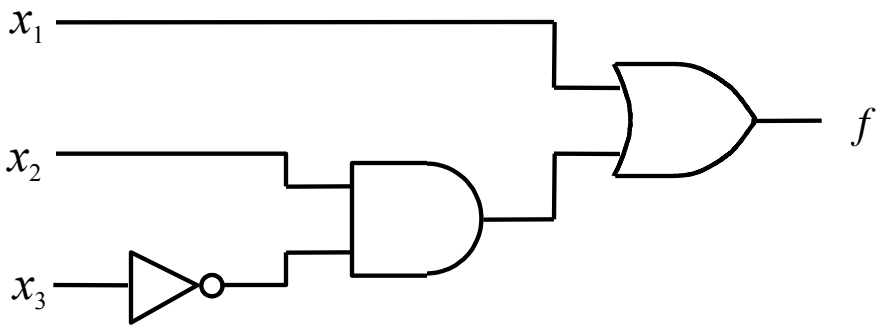


(a) POS implementation

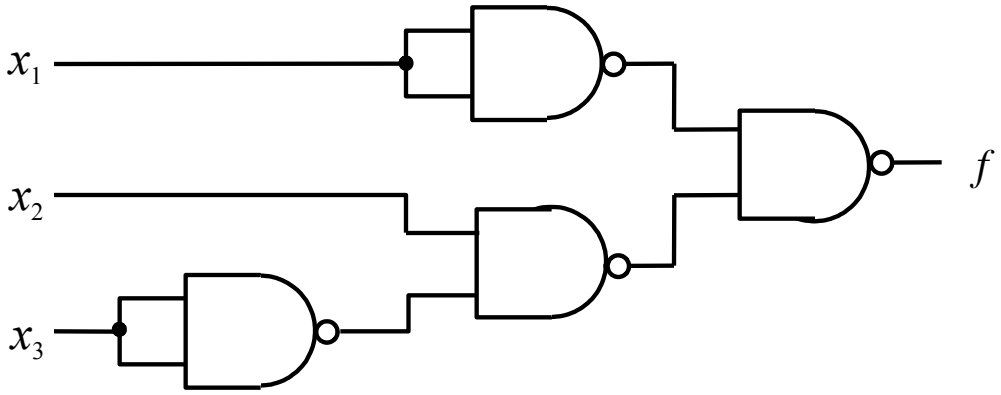


(b) NOR implementation

Figure 2.24 NOR-gate realization of the function in Example 2.6.



(a) SOP implementation

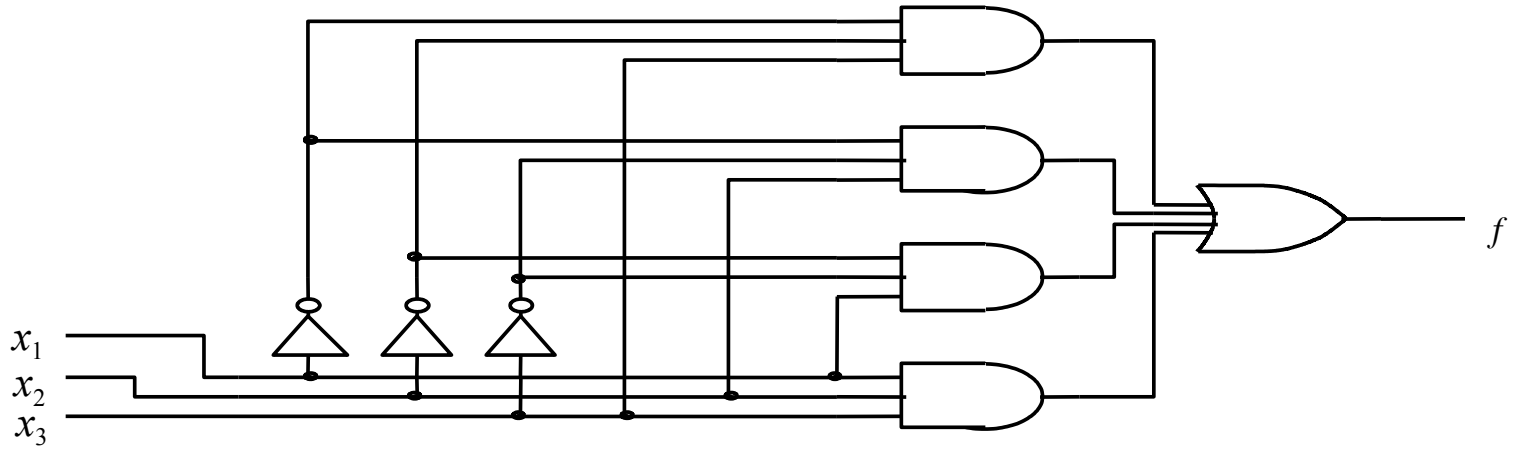


(b) NAND implementation

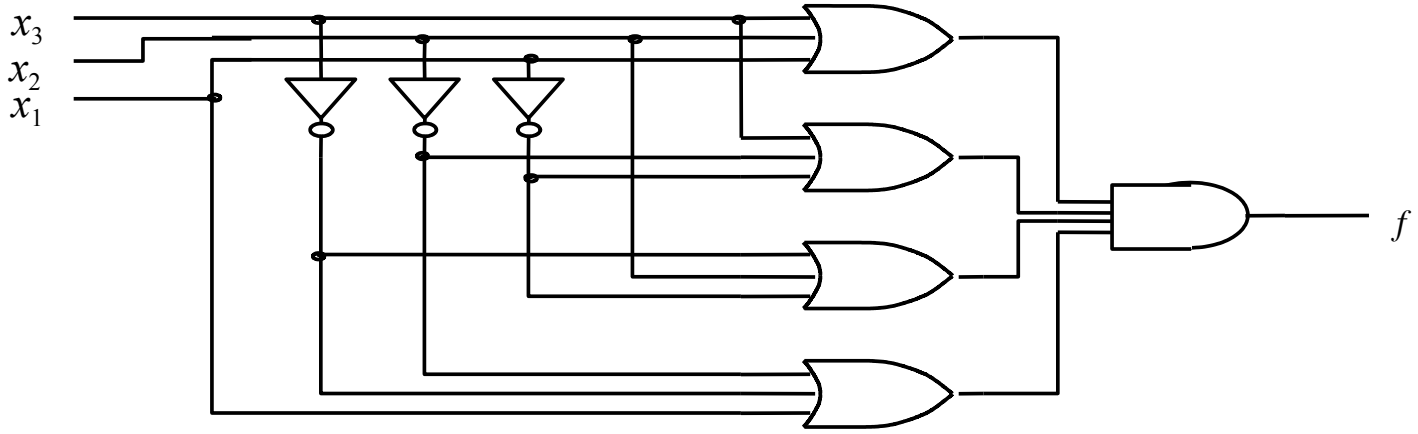
Figure 2.25. NAND-gate realization of the function in Example 2.7.

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 2.26. Truth table for a three-way light control.



(a) Sum-of-products realization

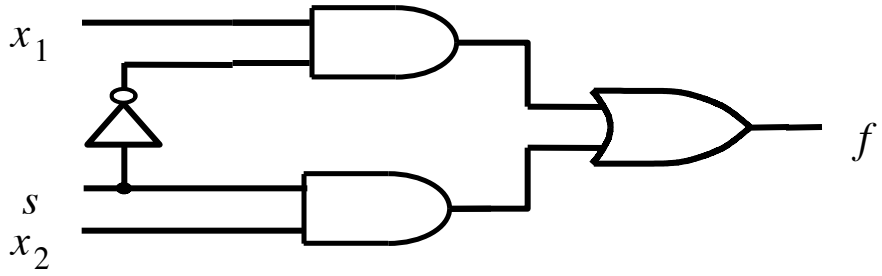


(b) Product-of-sums realization

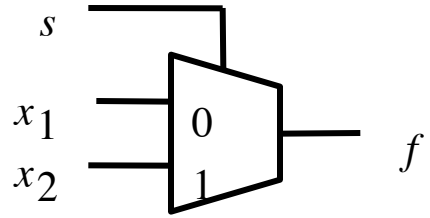
Figure 2.27. Implementation of the function in Figure 2.26.

s	x_1	x_2	$f(s, x_1, x_2)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(a) Truth table



(b) Circuit



(c) Graphical symbol

s	$f(s, x_1, x_2)$
0	x_1
1	x_2

(d) More compact truth-table representation

Figure 2.28. Implementation of a multiplexer.

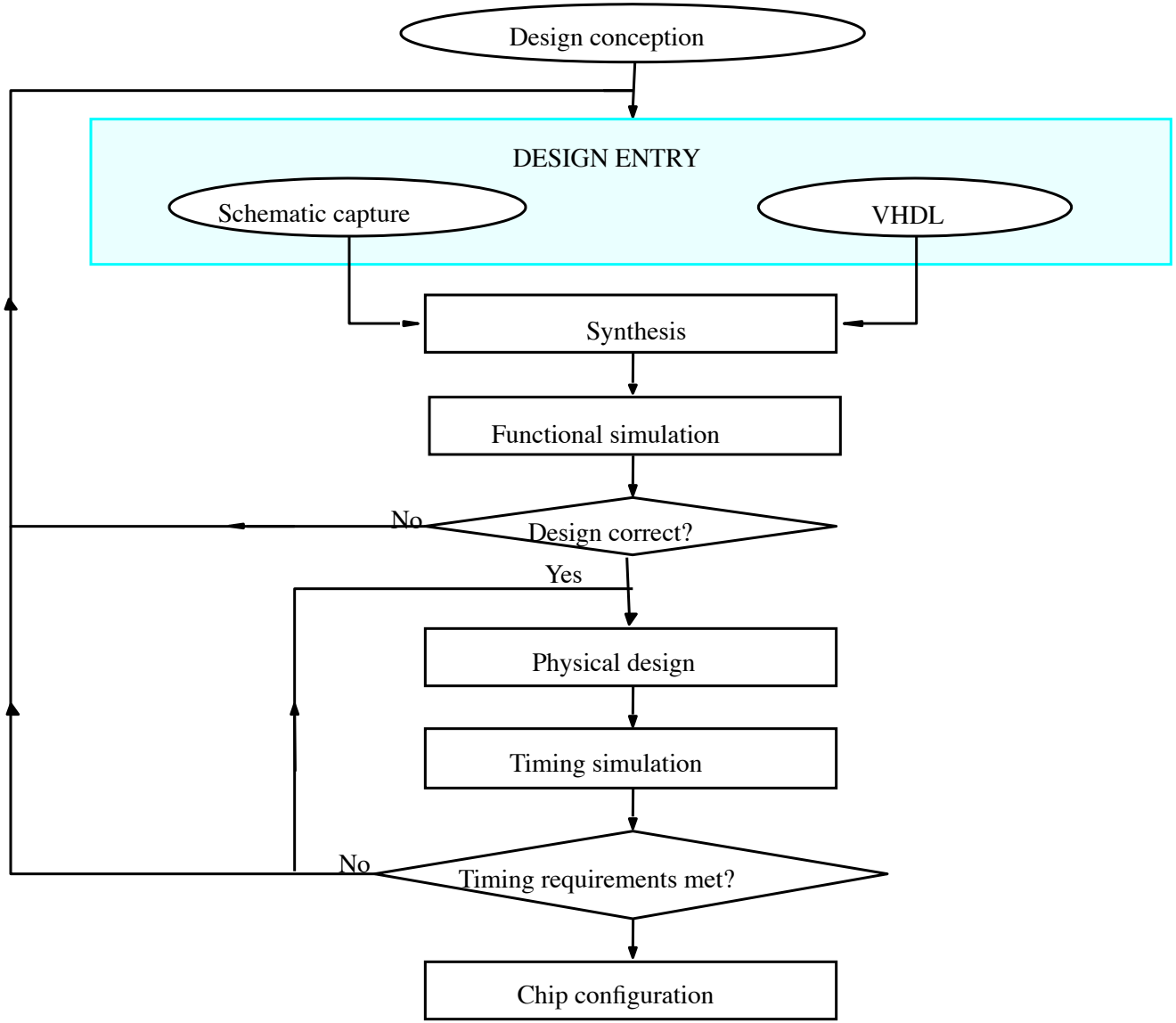


Figure 2.29. A typical CAD system.

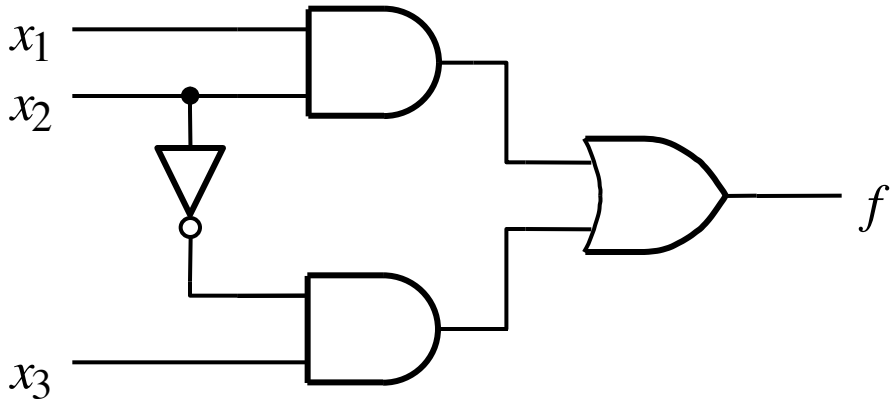


Figure 2.30. A simple logic function.

```
ENTITY  example1 IS
    PORT ( x1, x2, x3       : IN   BIT ;
           f                : OUT  BIT ) ;
END  example1 ;
```

Figure 2.31. VHDL entity declaration for the circuit in Figure 2.30.

```
ARCHITECTURE LogicFunc OF example1 IS
BEGIN
      f <= (x1 AND x2) OR (NOT x2 AND x3) ;
END LogicFunc ;
```

Figure 2.32. VHDL architecture for the entity in Figure 2.31.

```
ENTITY example1 IS
    PORT ( x1. x2. x3   : IN     BIT ;
           f            : OUT    BIT ) ;
END example1 ;

ARCHITECTURE LogicFunc OF example1 IS
BEGIN
    f <= (x1 AND x2) OR (NOT x2 AND x3) ;
END LogicFunc ;
```

Figure 2.33. Complete VHDL code for the circuit in Figure 2.30.

```
ENTITY example2 IS
    PORT ( x1. x2. x3. x4   : IN     BIT ;
           f. g             : OUT    BIT ) ;
END example2 ;

ARCHITECTURE LogicFunc OF example2 IS
BEGIN
    f <= (x1 AND x3) OR (NOT x3 AND x2) ;
    g <= (NOT x3 OR x1) AND (NOT x3 OR x4) ;
END LogicFunc ;
```

Figure 2.34. VHDL code for a four-input function.

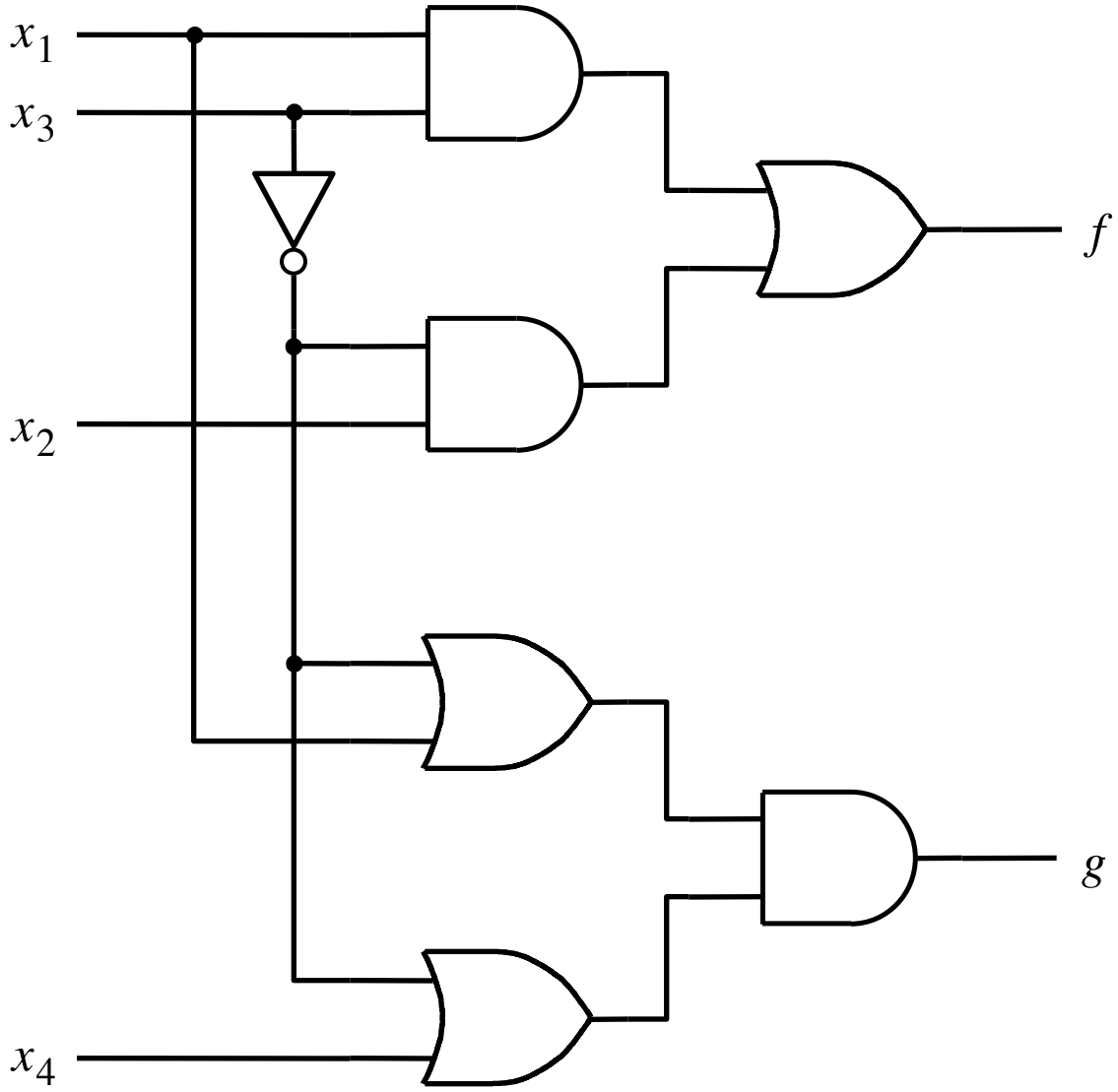
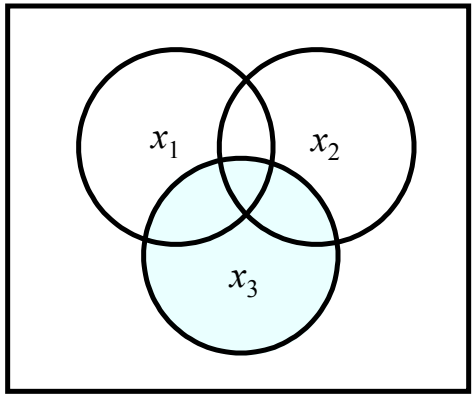
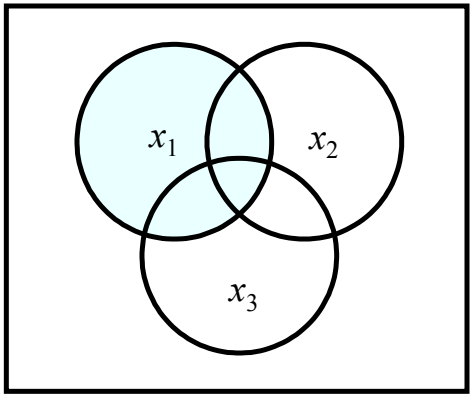


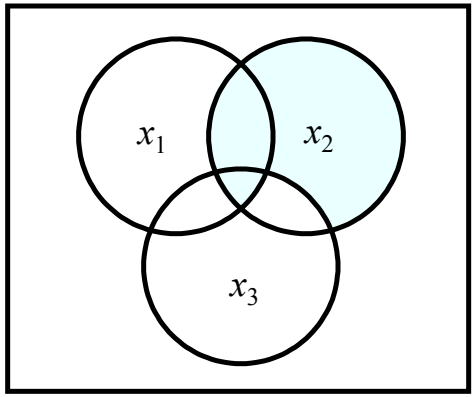
Figure 2.35. Logic circuit for the code in Figure 2.34.



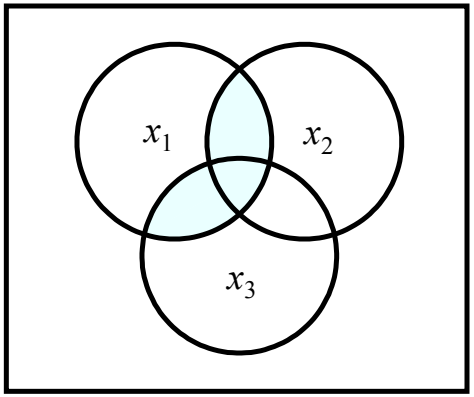
(a) Function *A*



(b) Function *B*



(c) Function *C*



(d) Function *f*

Figure 2.36. The Venn diagrams for Example 2.11.

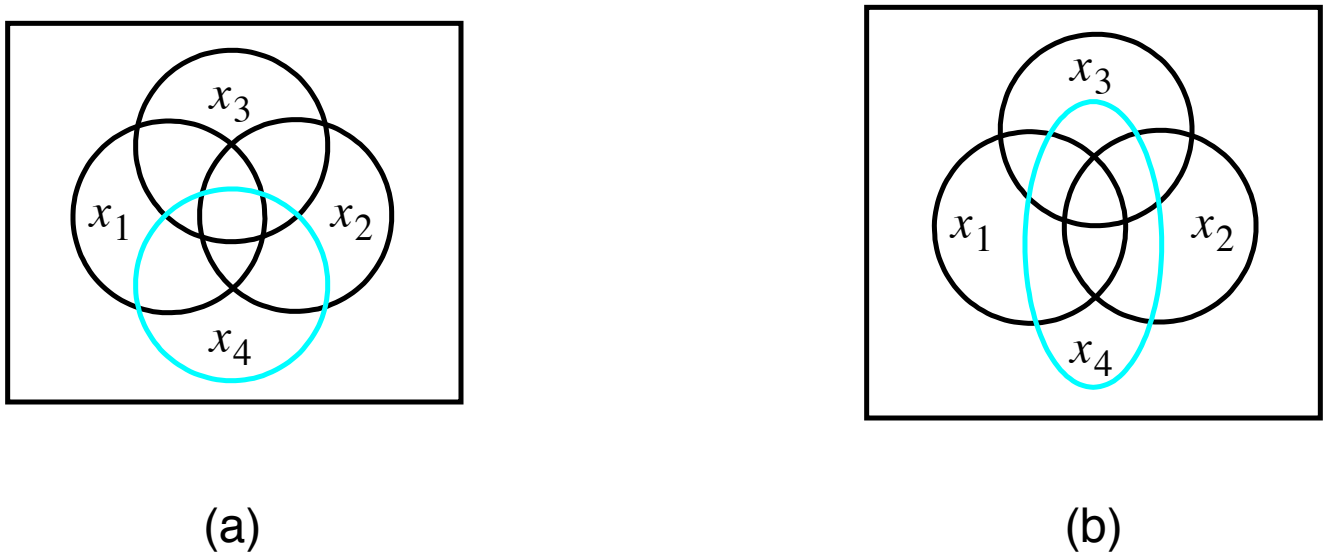


Figure P2.1. Two attempts to draw a four-variable Venn diagram.

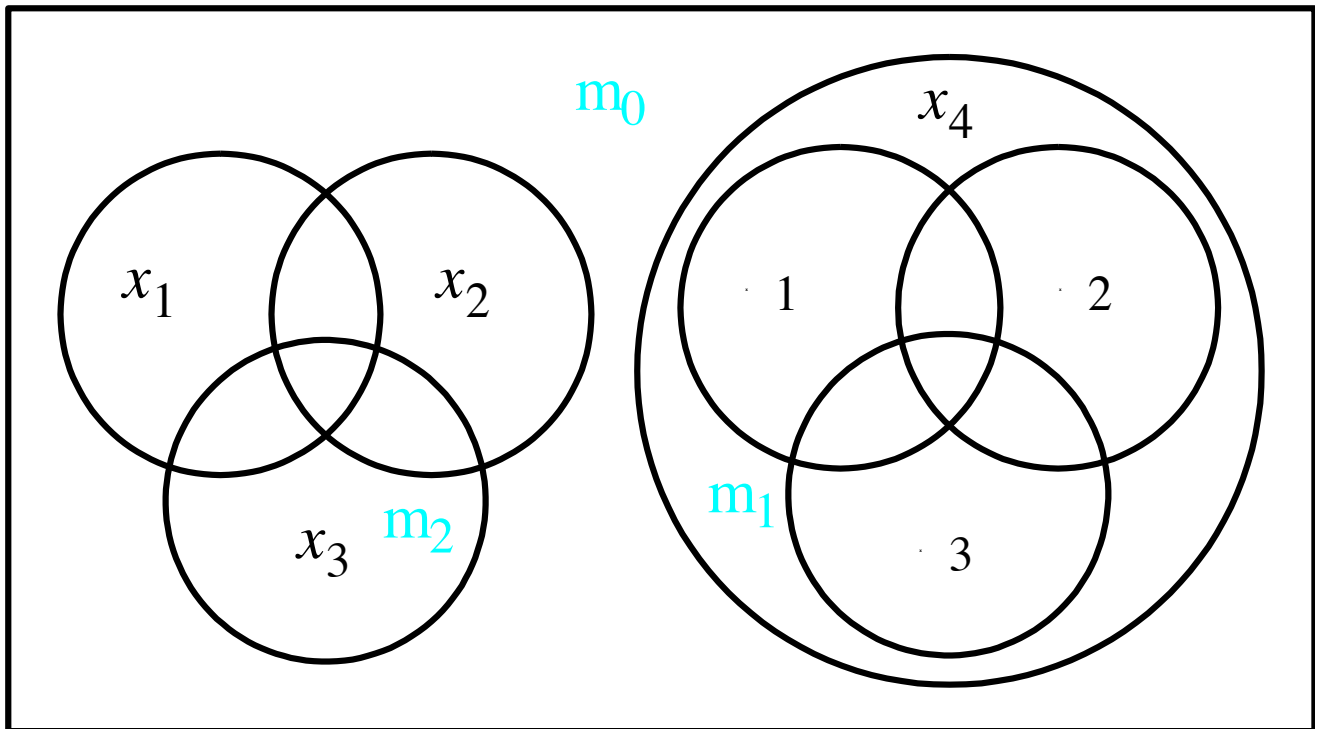


Figure P2.2. A four-variable Venn diagram.

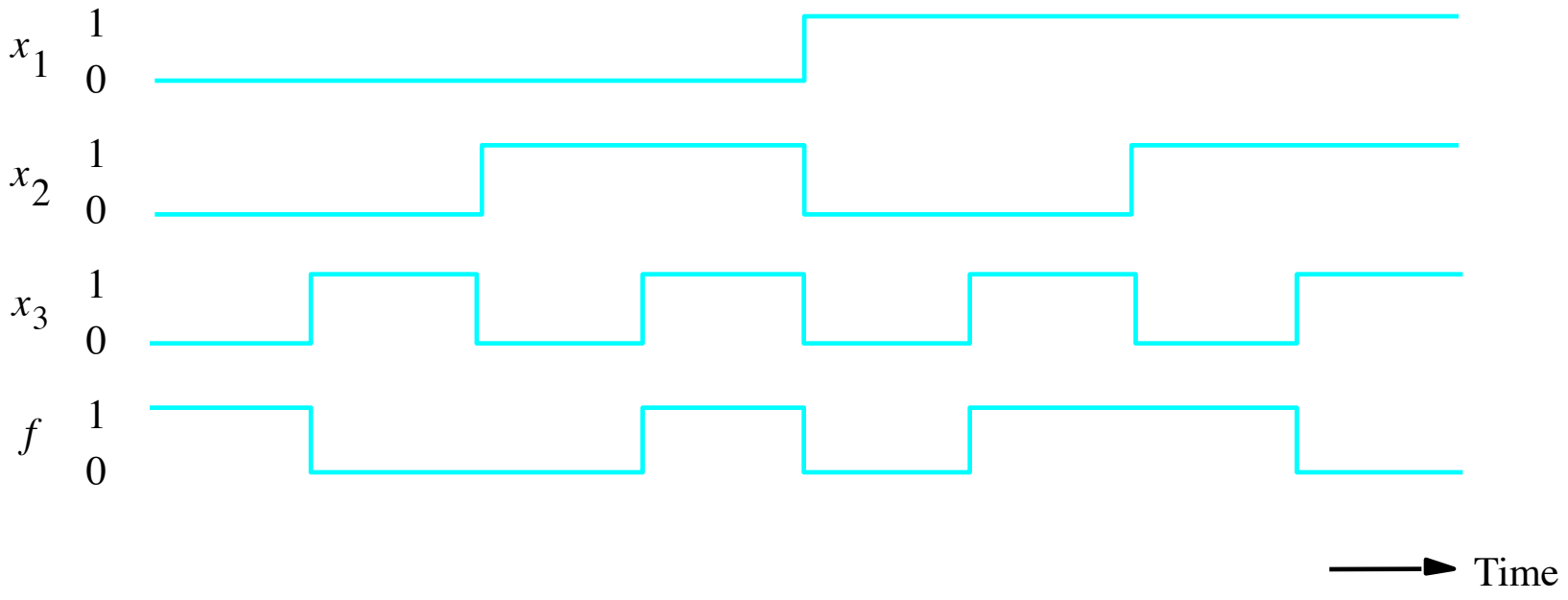


Figure P2.3. A timing diagram representing a logic function.

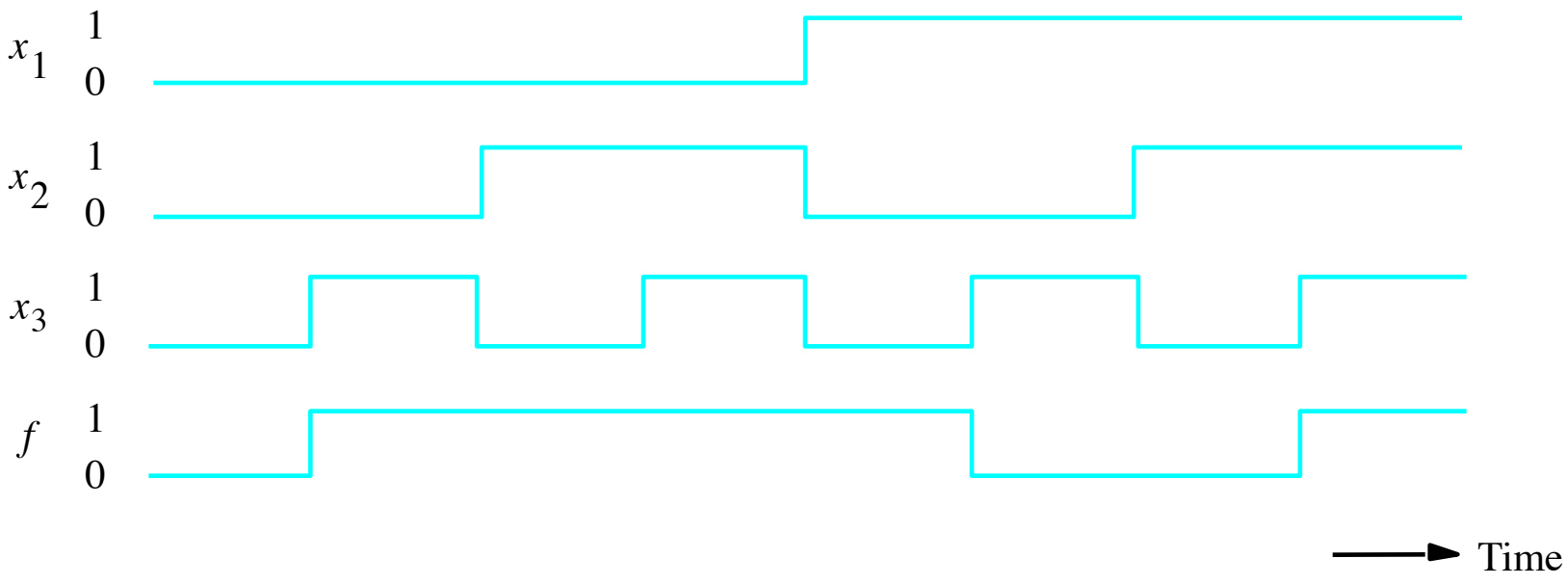


Figure P2.4. A timing diagram representing a logic function.